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Multi-Layered MoS_2 Thin Film Formed by High-Temperature Sputtering for Enhancement-Mode *n*MOSFETs

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Abstract

Multi-layered MoS_2 film of sub-10-nm formed by high-temperature sputtering has been investigated for enhancement-mode *n*MOSFETs. Raman peak of MoS_2 was observed even by using high-temperature sputtering. In addition, Hall mobility of sputtered MoS_2 film is obtained and it is considered that the enhancement-mode *n*MOSFETs could be realized through the decrease in carrier density and surface charge density.

1. Introduction

Molybdenum disulphide (MoS_2), one of the transition-metal dichalcogenides and has been used for solid lubricant so far, has attracted grate attention thanks to its wonderful characteristics such as flexibility, transparency and having energy band gap (E_g = 1.8 eV) [1]. In addition, MoS_2 has comparably high mobility (~700 $cm^2/V\cdot s$) even in thin region as shown in Fig. 1.

All of devices using MoS_2 so far have been depletion-mode and *n*-type. The reason of the depletion-mode operations are considered as unintentional n-type doping to the channel during the process of the production [1, 2]. K. Dolui, *et al.*, suggested that when Na atom is placed on the interface between SiO_2 and MoS_2, the electronic structure of the composite is strongly affected by the presence of Na ion and the system becomes *n*-type [3]. Therefore, in order to avoid Na contamination, the clean processes are needed to realize the enhancement-mode MoS_2 MOSFETs. In such phenomena, sputtering could be a candidate to realize enhancement-mode MoS_2 MOSFETs. Regarding sputtered MoS_2 has been already reported in a thicker region (~ 150 nm) for solid lubricant applications as following; high-temperature sputtering (300^{o}C) is the way to form horizontal MoS_2 film to the substrates [4].

In this study, sputtered thin MoS_2 film has been investigated in a thinner region for nanoelectronic devices.

2. Results and Discussion

Thin film of MoS_2 (five layers) parallel with the SiO_2 substrate could be available by using high-temperature sputtering (300^{o}C) as shown in Fig. 2. The substrate is heated up to 300^{o}C and MoS_2 is sputtered by RF magnetron sputtering. We found that ~10 nm thick MoS_2 film parallel with the substrate appeared and layers almost perpendicular to the substrate emerged near the surface, probably due to interface-morphology-related stress (Fig. 3). Fig. 4 shows the RMS roughness of sputtered MoS_2, which indicates 10 nm thick is the border of the thickness between horizontal and perpendicular layers to the substrate. Fig. 5 shows the Raman shift intensity normalized by Si intensity of the substrate. It indicates the increase in the Mo-S bonding amounts by introducing high-temperature sputtering. According to C. Lee, *et al.*, Raman shift peak difference between E^1_{2g} and A_{1g} modes decreases as with the thickness of exfoliated MoS_2 decreases [5]. However, the peak difference widened as with the thickness of sputtered MoS_2 decreased. It is considered as due to the increase in a value of roughness of sputtered MoS_2 film [6]. Fig. 7 shows the result of Hall measurements of sputtered MoS_2 film. Hall mobility of the film increased along with the thickness thinner because of the discontinuity of perpendicular region (>10 nm). In addition, carrier density (*n*-type) decreased compared to reported devices (ref. 7). Fig. 8 shows the simulated and reported threshold voltage. The simulation used the structure and the surface charge density (n_s) of ref. 2, and the carrier density of ref. 7. The results indicate that the mitigation of the carrier density and the surface charge density makes the threshold voltage plus, i.e., the device could be the enhancement-mode.

3. Conclusions

Thin film of MoS_2 was obtained by high-temperature sputtering and its carrier density is comparatively low compared to reported results. That fact shows the possibilities of realizing the enhancement-mode MoS_2 *n*MOSFETs with sputtering method. In order to achieve high mobility MoS_2 film, the improvement of the sputtered film quality will be the essential work in the future.

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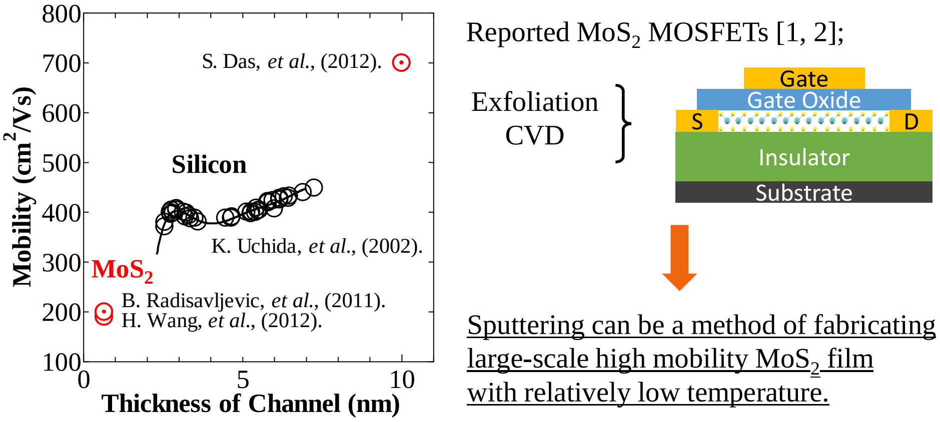
References

[1] H. Wang, *et al.*, *IEDM*, 4.6 (2012) 88-91.
[2] B. Radisavljevic, *et al.*, Nature Nanotech., **6** (2011) 147-150.
[3] K. Dolui, *et al.*, Physical review B **87** (2013) 165402.
[4] H. Moser and F. Levy, Mater. Res., **7** (3) (1992) 734-740.
[5] C. Lee, *et al.*, ACS NANO, **4** (5) (2010) 2695-2700.
[6] N.T. McDevitt, *et al.*, Thin Solid Films, **240** (1994) 76-81.
[7] B. Radisavljevic and A. Kis, Nature Mater., **12** (2013) 815-820.



(a) (b)

Fig. 1 Advantages of MoS_2 and sputtering method to fabricate MoS_2 film. When silicon, which is widely used for advanced LSIs, becomes thin film, the mobility deterioration will occur. In such region, MoS_2 has relatively high mobility. Sputtering method has good properties such as large-scale formation, low temperature (conventionally 650°C~ by CVD [1]) and commonly used process in LSIs production.

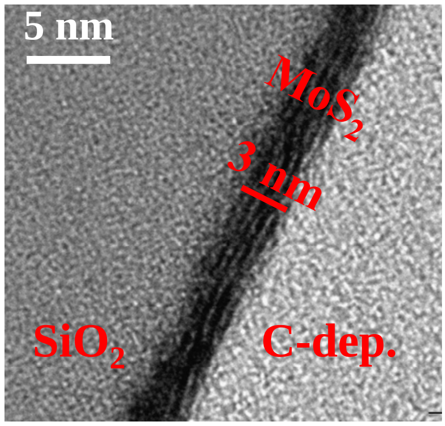


Fig. 2 TEM image of sputtered thin MoS_2 film. Five layers of MoS_2 film are seen. It is formed on SiO_2 substrate, therefore, it can be applied to the transistors of LSIs.

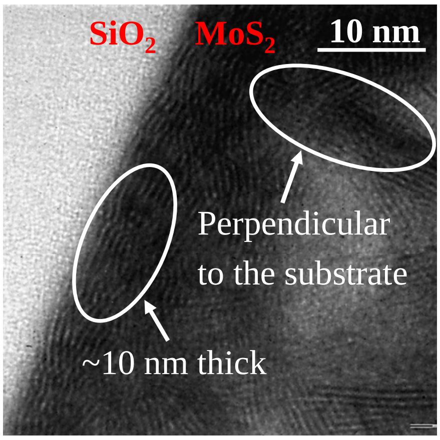


Fig. 3 TEM image of sputtered MoS_2. Two regions can be seen, one is horizontal layers and another is perpendicular layers to the interface.

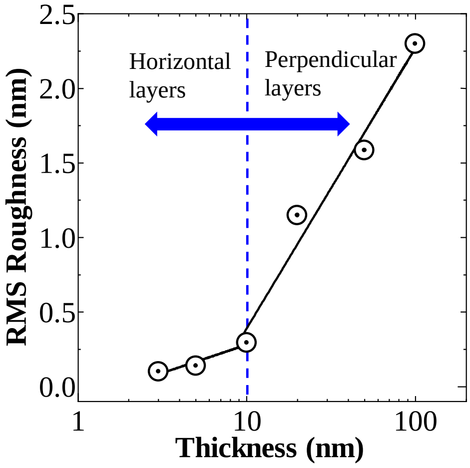


Fig. 4 RMS roughness of sputtered MoS_2 using AFM. Growth directions can be identified by changing the slope at 10 nm.

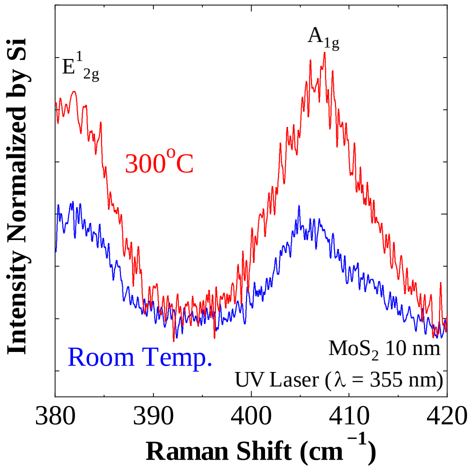


Fig. 5 Raman spectra of high- and room-temperature sputtered MoS_2 film (10-nm thick).

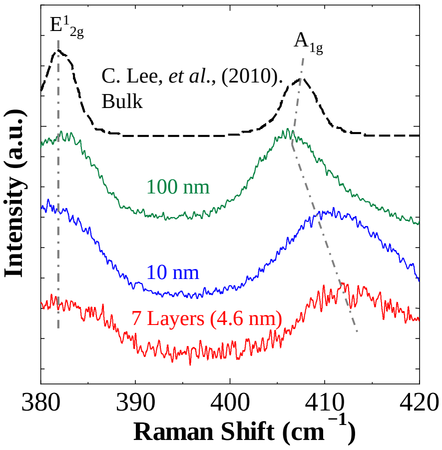


Fig. 6 Raman spectra of high-temp. sputtered MoS_2 on its thickness. As the thickness thinner, the difference between the peak of E^1_{2g} and A_{1g} narrows in usual. However, sputtered MoS_2 film performs opposite behavior with reported devices so far.

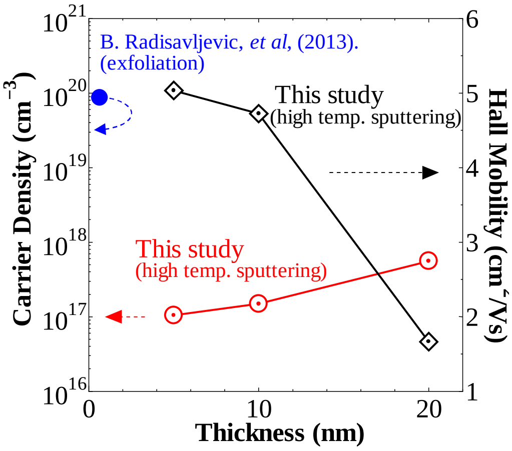


Fig. 7 Hall measurement results of high-temp. sputtered MoS_2. Carrier density (*n*-type) decreases compared to exfoliated film [7]. Thin film has relatively high mobility and low carrier density thanks to no perpendicular layers.

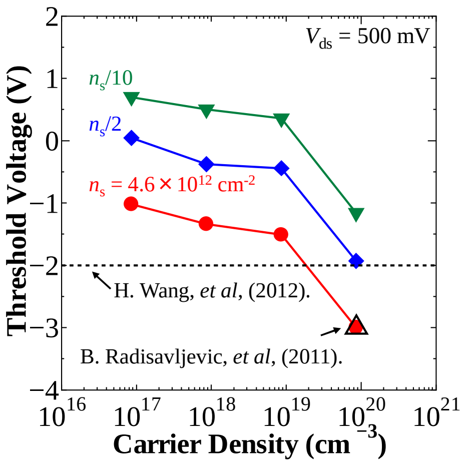


Fig. 8 Simulated threshold voltage dependence of *n*-type accumulation MOSFETs on carrier density and surface charge density (n_s) of MoS_2. This simulation used the structure, carrier density and surface charge deisnity in refs. 2 and 7.