# New Channel Materials and Devices Beyond Si CMOS

Peide D. Ye

School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University,
West Lafayette, IN 47906, U.S.A.
* Tel: 765-494-7611, Fax: 765-494-0676, E-mail: yep@purdue.edu

## 1. Introduction

Si CMOS is the single material and the single technology which dominates the microelectronics industry in the past decades. However, Si CMOS scaling is reaching its physical limit. Strained Si channel, high-k and metal gate, and 3D structure are the evolutionary technologies which might enough to keep Si CMOS scaling until 10nm node. Beyond 10nm, high mobility channel materials such as III-V and Ge are seriously considered to replace Si channel. The high mobility channels and their related dielectrics, contacts, substrate integrations are intensively investigated and evaluated currently by the major Si companies, academia and industrial consortia.

Interface is everything in MOS technology. Most of research in that front can be summarized as metal-semiconductor interface for source/drain contacts and oxide-semiconductor interface for dielectric gating. In this talk, we will review the state-of-the-art technology development in the recent years on III-V and Ge MOS technology by the industrial and academic leaders. Meanwhile, we will also report on some of new progress we made at Purdue University related with these two interfaces. Some of the highlights are listed following. By forming epitaxial high-k dielectric on GaAs (111)A surface by atomic layer deposition (ALD), we are able to demonstrate GaAs CMOS circuits, logic gates and ring oscillators for the first time after 50 years GaAs MOS research. By ALD high-k dielectric and metal gate, InGaAs gate-all-around (GAA) nanowire FETs offer high drain current, transconductance with subthreshold swing as low as 63 mV/dec. By recessed source/drain, high performance Ge nFETs are realized and the first Ge CMOS circuits are demonstrated on Si substrate.

At or even beyond 5nm node, the device channel must be atomic layer thin to avoid the short channel effects. The emerging 2D materials could be one of the solutions. Interface plays even more important role in these novel materials. We will focus on two 2D semiconducting materials – $MoS_2$ as n-type channel and phosphorene as p-type channel. We will present our newest results on $MoS_2$ with record high drain current and low contact resistance by the molecular chemical doping technique. We will also introduce the unique material properties of the newly pioneered p-type phosphorene and its potential for various device applications.

## 2. Experiments and Results

Here we list several experiments and results as examples. GaAs, as a typical III-V semiconductor, has long been considered to be a strong candidate to replace Si in future high-speed low-power logic applications.[1] In order to achieve a thermodynamically stable dielectric on GaAs with a low interface trap density, tremendous efforts have been made by different passivation techniques [2-5] since its first publication in 1965. [6] We previously reported high-performance GaAs nMOSFETs with single crystalline La-based oxide dielectrics. [7-8] In VLSI 2014, we demonstrate high-performance GaAs devices that are integrated into CMOS circuits (inverters, NAND and NOR logic gates, and five-stage ring oscillators). These devices were enabled by the high-quality interface of single-crystalline $La_2O_3$ grown on GaAs(111)A by atomic layer epitaxy. [9] Mid-gap interface trap density ($D_{it}$) as low as $2\times10^{11}/cm^2$-eV is achieved.

III-V MOSFETs have been considered promising candidate for post-Si logic devices beyond 10nm technology node. [1] Recently, a top-down technology for III-V GAA nanowire MOSFETs has been demonstrated to improve the electrostatic control of the channel based on good progress of planar InGaAs MOSFETs.[10] In IEDM 2012, we experimentally demonstrate InGaAs GAA nanowire MOSFETs with an EOT down to 1.2nm by the successful integration of higher-k dielectric $LaAlO_3$ (k~16).[11] The reduction of EOT has allowed the demonstration of the first 20nm $L_{ch}$ InGaAs MOSFETs with $g_m$ of 1.65mS/μm at $V_{ds}$=0.5V and negligible short channel effects (SCE). A systematic scaling metrics study with $L_{ch}$ between 20-80nm and nanowire size-dependent transport study with nanowire width ($W_{NW}$) between 20-35nm has also been carried out, demonstrating volume inversion and a near-ideal SS of 63mV/dec and DIBL of 7mV/V. It is shown that the integration of 4nm $LaAlO_3$ with ultra-thin 0.5nm $Al_2O_3$ interfacial layer allow reduction of EOT=1.2nm with optimized $D_{it}$, offering excellent scalability, near-ballistic transport, and high $g_m$ at low supply voltage. There are many excellent III-V MOSFET work reported in the past years. [12-18]

Low resistivity Ge n-contacts and high performance Ge nMOSFET is difficult to realize because the Fermi-level tends to be pinned to Ge valence band edge. [19-23] In VLSI 2013, we report the world's first demonstration of Ge CMOS technology based on a recessed junctionless (JL) approach. nFETs and pFETs are successfully integrated on a GeOI substrate. A novel recessed S/D method is invented and greatly enhances n-Ge contact, based on which nFETs as short as 25 nm and record large on current of 544 mA/mm are achieved. [24] Based on this progress on Ge nFETs, we will report the first experimental demonstration of Ge CMOS circuits in IEDM 2014. Ultra-scaled Ge CMOS logic devices with channel lengths ($L_{ch}$) from 500 to 20 nm, channel thicknesses ($T_{ch}$) of 25 and 15 nm, EOTs of 4.5 and 3 nm and a small width ratio

($W_n$:$W_p$=1.2) are realized on a GeOI substrate. The CMOS inverters have high voltage gain of up to 36 V/V, which is the best value among all of the non-Si CMOS by the standard top-down approach. Scalability studies on Ge CMOS inverters down to 20 nm are carried out for the first time. NAND and NOR logic gates are also investigated.

The rise of two-dimensional (2D) crystals has given new challenges and opportunities to the device research. Transition metal dichalcogenides (TMDs), typically $MoS_2$, show good potentials in device applications due to a satisfied band gap compared to graphene, thermal stability, carrier mobility, and compatibility to silicon based CMOS process. [25,26] In order to realize high-performance $MoS_2$ MOSFETs, three major issues need to be completely addressed: how to achieve a high-quality interface between 2D crystal and dielectric, how to achieve a low-resistivity metal-semiconductor junction, and device performance at scaled dimensions. Although the high-k dielectric has been successfully demonstrated previously, the interface quality between high-k dielectric and 2D crystal needs to be systematically studied. High-k dielectric thickness needs to be scaled along with the channel length and width. Secondly, as the material cannot be effectively implanted due to the ultrathin nature, the contact resistance ($R_c$) is mostly determined by the Schottky barrier at the $MoS_2$/metal interface. Contact metal and doping engineering are needed to realize low resistivity contacts so that high performance 2D FETs can be demonstrated. The third issue is related with transistor dimension, which determines the packing density for a single chip. For potential applications, the performance limitation of $MoS_2$ transistors associated with channel length/width scaling must be investigated. Due to the surphur vacancy or charge neutral level of metal/$MoS_2$ interface located at the vicinity of the conduction band edge, $MoS_2$ FETs perform as n-channel Schottky barrier transistors. Black phosphorus (BP) and phosphorene, complementing to $MoS_2$, is a p-type channel material. It provides a good addition to the existing 2D family and great opportunities for 2D hetero-structures and hetero-integrations. Two important building blocks for modern microelectronics, CMOS and PN diode, are demonstrated using $MoS_2$ as n-type and BP as p-type materials.

We demonstrate high-performance $MoS_2$ FETs with record drain current of 460 mA/mm and record low contact resistance of 0.5 Ω·mm enabled by molecular chemical doping of 1,2 dichloroethane (DCE). [27] We introduce a new p-type 2D material called phosphorene which is one monolayer of layered BP. [28,29] At room temperature, the few-layer phosphorene field-effect transistors with 1.0 μm channel length display a high on-current of 194 mA/mm, a high hole field-effect mobility of 286 $cm^2/V{\cdot}s$, and an on/off ratio up to $10^4$. We demonstrate the possibility of phosphorene integration by constructing the first 2D CMOS inverter of phosphorene PMOS and $MoS_2$ NMOS transistors and the first BP/$MoS_2$ PN diode for photonic applications. [26]

## 3. Conclusion

New materials and structures become more and more important in device research beyond traditional Si CMOS. We review the significant progress on high mobility channel materials and devices research in the past years showing the promise of using III-V and Ge in future CMOS logic application. We use $MoS_2$ and phosphorene as examples to show that well-behaved transistors can be demonstrated on these van der Waals 2D materials for both n-type and p-type channels. To compete with the existing transistor technology, much more efforts are needed in dielectric integration, contact engineering, scaling research. We also demonstrate the feasible way to integrate n-type and p-type 2D materials on the same platform to form CMOS and PN diodes and their potentials for future microelectronics and photonics applications.

## Acknowledgment

Most of the experiments presented here were performed by the postdocs and Ph.D. students working in my group in the past 10 years. They are Yi Xuan, Yanqing Wu, Jiangjiang Gu, Min Xu, Ling Dong, Adam Neal, Han Liu, Yexin Deng, Yuchen Du, Nathan Conrad and others. We thank our collaborators at Purdue, Harvard, UT Dallas, Lehigh, Rice and MSU for their support. The work at Purdue was sponsored by NSF, AFOSR, ARO, SRC, SEMATECH, Intel, IBM and SRC FCRP MSD Center.

## References

[1] J.A. del Alamo, *Nature*, **479** (7373), 317−323, 2011.
[2] M. Hong *et. al*., *Science*, **283**, p. 1897, 1999.
[3] M. Passlack *et al.*, *Appl. Phys. Lett.*, **68**, p. 1099, 1996.
[4] P.D. Ye *et al.*, *Elec. Dev. Lett.*, **24**, p. 209, 2003.
[5] R.J.W. Hill *et al.*, *Elec. Dev. Lett*. 28, p. 1080, 2007.
[6] H. Beche, *et al*., *Solid-State Electron*, **8**, 813, 1965.
[7] L. Dong, *et al.*, *Elec. Dev. Lett.* **34**(4), p. 487, 2013.
[8] X.W. Wang, *et al.*, *Nano Lett*.**13**(2), p. 594, 2013.
[9] L. Dong *et al.*, *VLSI Tech. Dig.*, p.50, 2014.
[10] J. Gu *et al.*, *IEDM Tech. Dig.*, p.769, 2011.
[11] J. Gu *et al.*, *IEDM Tech. Dig.*, p.663, 2012.
[12] G. Dewey *et al.*, *Elec. Dev. Lett*. **29**(10), p. 1094, 2008.
[13] M. Radosavljevic *et al.*, *IEDM Tech. Dig.*,33.1,2011.
[14] D.-H. Kim, *et al.*, *IEDM Tech. Dig.*,p.761,2012.
[15] N. Taoka, *et al.*, *IEDM Tech. Dig.*,27.2 ,2012.
[16] M. Rodwell *et al.*, *IPRM*, p.9, 2007.
[17] M. Egard *et al.*, *IEDM Tech. Dig.*, p.303, 2011.
[18] Y. Yonai *et al.*, *IEDM Tech. Dig.*,p.307, 2011.
[19] J. Mitard, *et al.*, *VLSI Tech. Dig.*, p.82, 2009.
[20] B. Duriez, *et al.*, *IEDM Tech. Dig.*, p.522, 2013.
[21] S. Takagi, *et al.*, *IEEE Trans. Elec. Dev.*, p.21, 2008.
[22] A. Tourimi, *et al.*, *IEDM Tech. Dig.*, p.646, 2011.
[23] K. Martens *et al.*, *Appl. Phys. Lett.*, p.13504, 2011.
[24] H. Wu *et al.*, *VLSI Tech. Dig.*, p.76, 2014.
[25] B. Radisavljevic *et al.*, *Nat. Nanotechnol.* **6**, 147, 2011.
[26] H. Liu, and P. D. Ye, *IEEE Elect. Dev. Lett.* **33**, 546, 2012.
[27] L. M. Yang, *et al.*, *VLSI Tech. Dig.*, p.192, 2014.
[28] H. Liu, *et al.*, *ACS Nano* **8**, p.4033, 2014.
[29] L. Li, *et al.*, *Nature Nanotechnology* **9**, p.372, 2014.
[30] Y. Deng, et al., *ACS Nano* **8**, 10.1021/nn5027388, 2014.