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High mobility ultrathin GeSn (111) pMOSFETs by solid phase epitaxy

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Abstract

We have fabricated ultrathin GeSn(111) layers on Si by solid phase epitaxy (SPE) of amorphous GeSn layers, and demonstrated the depletion-mode operation of GeSn pMOSFETs. It is found that the mobility of the GeSn channel increases for increasing Sn concentration.

1. Introduction

GeSn has been predicted to exhibit carrier mobilities exceeding both that of Ge and Si, which makes GeSn suitable as alternative channel material in high-speed Si CMOS technology [1]. For the heterogeneous integration of GeSn channels into Si CMOS, an appropriate fabrication technology of single crystalline GeSn layers on Si wafers is required. Recently, we realized high quality GeSn layers directly on Si(111) substrates using solid phase epitaxy (SPE) of amorphous GeSn layers, indicating the potential of GeSn MOSFET devices on Si [2]. In this study, we fabricate ultrathin GeSn layers on Si(111) substrates by SPE, with Sn concentration of 6.75%, 4.5% and 0%. We investigates the electrical performance of ultrathin GeSn layers as a channel material in the depletion-mode GeSn pMOSFETs on Si substrates.

2. Experiment

Ultrathin p-type GeSn layers directly on Si have an appropriate band structure for depletion-mode pMOSFET devices, owing to the decent valence band offset between Si and GeSn, which helps localizing holes into GeSn channel (Fig. 1). By applying a negative gate voltage, a hole accumulation layer is formed at the interface and majority hole carriers are present both at the MOS interface and within the GeSn layer. When a positive gate voltage is applied, holes are electrostatically depleted, resulting in a reduction in the drain current. In order to fully deplete the channel of carriers, the off-state could be achieved by reducing the channel thickness below the maximum depletion layer width.

As an ultrathin channel, 5.0 nm amorphous GeSn (Sn concentration; 0, 4.5, and 6.75%) layers and 2.5 nm Ge cap layers are deposited on high resistivity Si substrates with (111) orientation. Subsequent annealing at 600˚C for 1 minute in N_2 ambient transforms the amorphous GeSn into a single crystalline layer by SPE. Then, GeSn pMOSFETs is fabricated with TaN/Al_2O_3 gate stack and self-aligned NiGeSn metal S/D. The process procedure and the device structure are indicated in Fig. 2. Figure 3 show the high resolution transmission electron microscopy (TEM) cross section images of fabricated ultrathin Ge and GeSn(6.75%) pMOSFETs. After the fabrication process, uniform Ge and GeSn layer with a thickness of around 5.5 nm is observed with sharp interfaces between the layers and both the Al_2O_3 gate dielectric and Si substrate. We could not observe any Sn segregation in the whole area of GeSn channel because of the low temperature fabrication process.

3. Results and discussion

Figure 4 show Id-Vg characteristics of ultrathin GeSn pMOSFETs for a gate length Lg = 100μm, with logarithmic and linear scale. All devices show good transfer characteristics. On/off ratio of 10^3 is achieved thanks to the ultrathin GeSn layer which thickness is thinner than its maximum depletion layer width. The on current increases significantly with increasing Sn concentration at the same gate overdrive. These results indicate the successful operation of depletion-mode GeSn pMOSFETs directly on Si, without insulating box layer. Id-Vd characteristics also indicate the current gain of nearly 100% for the 6.75% GeSn layer compared to the pure Ge layer (Fig. 5). We compare the mobility of the transistors with different Sn concentration (Fig. 6). Pure Ge sample suggests higher hole mobility in respect with p-type bulk Si ($Na = 4 \times 10^{18} cm^{-3}$). For increasing Sn concentration, we observe hole mobility enhancement. Compared with with pure Ge channel (0% Sn), GeSn MOSFETs with 4.5 and 6.75% Sn indicate hole mobility enhancements approximately up to +25 and +90%, respectively, attributed to increasing substitutional Sn incorporation in Ge. We also validate that the quality of ultrathin GeSn layers fabricated by the SPE method is sufficiently high to provide high mobility GeSn MOSFET performance.

4. Conclusions

In conclusion, we have demonstrated a depletion-mode pMOSFET using ultra-thin (5.0 nm) GeSn(111) channel on Si. The devices using SPE show good transfer

characteristics with an On/Off ratio of more than 1000 thanks to the ultrathin GeSn layer with thickness below the maximum depletion layer width. The GeSn(6.75%) layer sample shows around 90% improvement in hole mobility in respect with a pure Ge channel.

Acknowledgements

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A part of the device fabrication was carried out at AIST-NPF.

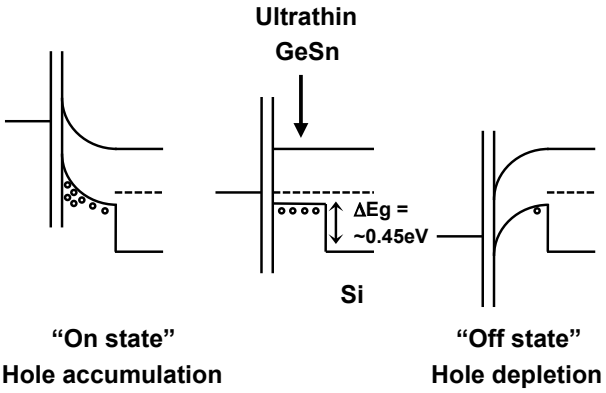

Fig. 1 Energy band diagrams for the depletion-mode pMOSFET operation using ultrathin GeSn channel directly on Si.

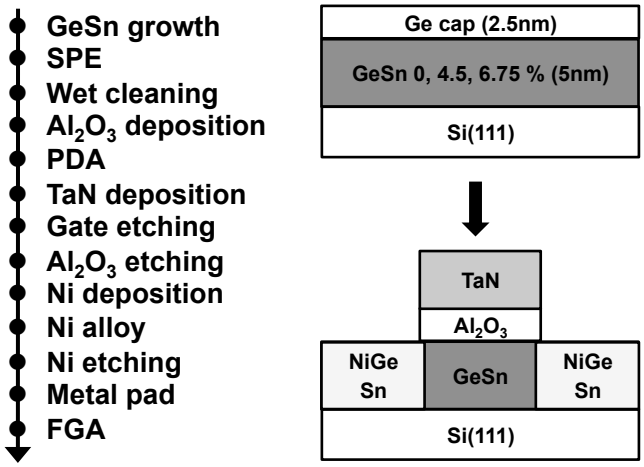

Fig. 2 Process flow and schematics of GeSn SPE and GeSn pMOSFETs

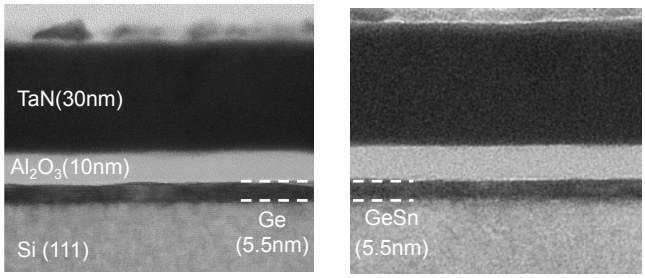

Fig. 3 Cross-section TEM images of ultrathin Ge and GeSn(6.75%) (111) pMOSFETs

References

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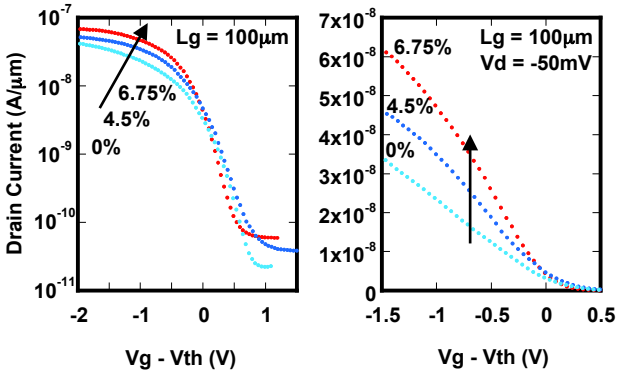

Fig. 4 Id-Vg characteristics of ultrathin GeSn pMOSFETs for a gate length Lg = 100μm with logarithmic and linear scale, measured at a drain voltage of -50 mV.

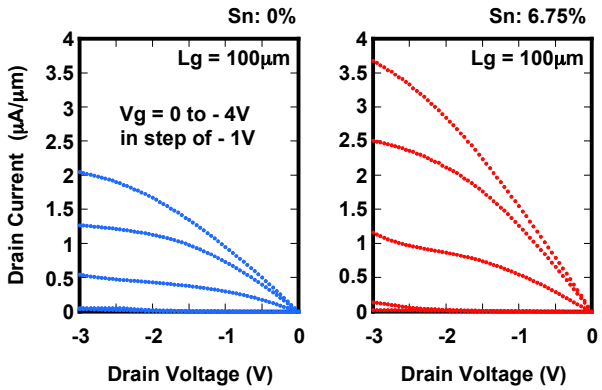

Fig. 5 Id –Vd characteristics for ultrathin Ge and GeSn pMOSFETs with Sn concentration of 0 and 6.75%.

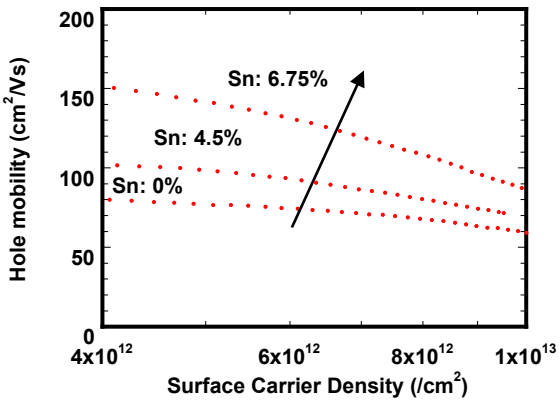

Fig. 6 Hole mobility for ultrathin Ge and GeSn pMOSFETs measured using split CV method.