Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials, Tsukuba, 2014, pp24-25

Recovery of Interface States Generated by Hot-Carrier Stress

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Abstract

Interface states (N_{it}) generated by hot-carrier stress were investigated in detail. ΔN_{it}, which is usually considered to be unrecoverable, exhibited recovery under high-temperature conditions. This recovery could be expressed using an empirical equation, and interestingly, showed universality. These features can be interpreted by the activation energy distribution of N_{it} annihilation. The possible origins of N_{it} are the well known P_b-centers (interfacial Si dangling bond) and interfacial bulk traps. The N_{it} generation/recovery model was also proposed.

1. Introduction

With the scaling down of metal-oxide-semiconductor field effect transistors (MOSFETs), the impact of hot-carrier stress (HCS) has become more prominent. Hot-carrier stress induces the generation of interface states (N_{it}) and bulk traps (N_{ot}). There have been many studies on the N_{it} generation process [1], while there have been few on annihilation (i.e., ΔN_{it} recovery). However, since modern MOSFETs are often operated under high-temperature conditions, there is a possibility that the recovery of ΔN_{it} formed by HCS has a certain effect on MOSFET characteristics. Therefore, the mechanism of ΔN_{it} recovery should be investigated for understanding MOSFET physics as well as the simulation of MOSFET characteristics. In this study, the recovery mechanism of ΔN_{it} by HCS under high-temperature conditions was investigated in detail.

2. Experiments

The samples used in the experiments were p- and nMOSFETs with 5-nm-thick SiO_2 gate insulators (L/W=0.25/15 μm). The HCS stress conditions are summarized in Table I.

The isothermal annealing technique, isochronal annealing and maximum entropy method (IAMEM) [2], and spin-dependent recombination (SDR) methods [3] were applied to confirm ΔN_{it} recovery, determine activation energy distribution of ΔN_{it} recovery (E_a) [2], and identify N_{it} origins. The amount of ΔN_{it} was determined using the DCIV method. Annealing schemes are depicted in Fig. 1 and Table II. The SDR signals (spin-dependent DCIV peak currents) were measured with X-band electron spin resonance equipment [3].

3. Results and Discussion

The ΔN_{it} in $pMOS^{CHC}$ during isothermal annealing is shown in Fig. 2(a). At T_r=373K, ΔN_{it} exhibited subtle decrease even after long t_r, while significant recoveries were clearly observed at higher T_r. Grasser *et al*. suggested that ΔV_{th} recovery after negative bias temperature stress can be expressed using the empirical equation $\Delta V_{th}(t_r)=R+P=C/\{1+B(t_r/t_s)^{\beta}\}+P$, where R denotes the recoverable component, P is a constant for the permanent component, and C, B, β are fitting parameters [4]. Referring to their study, ΔN_{it} recovery can be expressed as

$$\Delta N_{it}(t_r)=R+P=C/\{1+B(t_r/t_s)^{\beta}\}+P. \quad (1)$$

The lines in Fig. 2(a) are the fitting results from Eq. (1). Good reproducibility proves the validity of this equation. The P values suggest that ΔN_{it} includes both R and P at low T_r, while only R dominates ΔN_{it} at high T_r. The R and P can be extracted distinguishably from these fittings.

The scaled Rs of all MOSFETs are compared in Fig. 2(b). At T_r=373K, the Rs of $pMOS^{CHC}$ and $nMOS^{DAHC}$ (group X) ($nMOS^{CHC}$ and $pMOS^{DAHC}$ (group Y)) agreed well, while those of groups X and Y showed deviations. At T_r=473K, the all Rs became different. Interestingly, at T_r=573 and 623K, they became almost equal (universality).

To interpret these R behaviors, IAMEM experiments were carried out [2]. Figure 3(a) is $\Delta N_{it}(T_a)$ and $\Delta V_{th}(T_a)$ of $pMOS^{CHC}$. They decreased with T_a, due to the temperature accelerated recovery. Figure 3(b) shows $\Delta V_{th}(T_a)$ as a function of $\Delta N_{it}(T_a)$. This plot reveals the polarity of N_{ot} as follows. When ΔN_{ot} can be ignored, $\Delta V_{th}(T_a)$ is proportional to $\Delta N_{it}(T_a)$ [5]. Because the proportionality was observed at the high T_a region, ΔV_{th} was dominated only by ΔN_{it} at high T_a, while ΔV_{th} at low T_a was composed of ΔN_{it} and ΔN_{ot}. The experimental points at low T_a are located above the proportional line, suggesting that the N_{ot} is a hole trap.

The IAMEM results (E_a) and N_{ot} polarities are shown in Fig. 4. Interestingly, there are several peaks (A, A', and B). As mentioned above, all the recovery curves were well reproduced $R+P$. Only peaks A and A' can recover at low temperature because their E_a are low, while peak B, which appears at high E_a, can recover at high temperature. Therefore, it is reasonable to assume that at low temperature, R and P are due to the recoveries of peaks A(A'), and peak B, while R arises from the recovery of peak B at high temperature (note that P=0 at high temperature). The E_a of peaks A of $pMOS^{CHC}$ and $nMOS^{DAHC}$ (group X) were coincident and at low temperature (T_r=373K), peaks A can recover, while peaks B can not. Therefore, the scaled Rs of $pMOS^{CHC}$ and $nMOS^{DAHC}$ in Fig. 2(b) became almost equal at T_r=373K. Similar discussion can be applied regarding the

E_a of peaks A' of nMOS^{CHC} and pMOS^{DAHC} (group Y). At T_r=473K, the scaled Rs of all MOSFETs were not coincident because both peaks A (A') and B can recover and have an effect on R. At T_r=573 and 623K, since all Rs arise from peaks B that have the same E_a, they became equal. This is the reason of universality observed in the recovery.

The origin of traps are now discussed. Two peaks were observed in the SDR spectra (Fig. 5). They can be considered to be P_{b0}- and P_{b1}-centers (Si_3≡Si· located at the interface, where · denotes a dangling bond) from their g-values [6]. The E_a of the P_b-centers were determined to be about 1.7 eV [7], meaning that the P_b-centers caused peaks B in Fig. 4. Although no other peaks corresponding to peaks A and A' in Fig. 4 were observed in Fig. 5 within experimental errors, we believe that peaks A and A' were due to ΔN_{ot} (hole) near the interface [1]. Note that ΔN_{it} was measured using DCIV, which can detect any interfacial traps including N_{ot} acting as a recombination center. A possible candidate is the E'-center (O_3≡Si·) [1]. Note that although only the SDR of pMOS^{CHC} was discussed in this paper, the SDR of other MOSFETs provided the same results.

Based on these results, the model of the generation/recovery of ΔN_{it} is introduced. During HCS, the carriers break the interfacial Si-H bonds and the bulk Si-O bonds, leaving P_b-centers and E'-centers [1], respectively. After HCS, the captured carriers at the E'-center are emitted and at the same time, the broken Si-O bonds are re-formed. As a result, E'-centers are diminished. These processes can occur even at low temperature and correspond to peaks A and A' in Fig. 4. On the other hand, the emitted H moves back toward the interface and passivates the interfacial Si·, resulting in the recovery of the P_b-centers. This passivation occurs only at high temperature and provides peak B in Fig. 4. This model can explain the experimental results well; however, there are still several issues, e.g., the origin of N_{ot}, and further examination is required.

4. Conclusions

The N_{it} induced by HCS was examined through recoveries. The degradation in pMOS^{CHC} and nMOS^{DAHC} arise from hole N_{ot} and two P_b-centers, while electron N_{ot} and P_b-centers result in the degradation of nMOS^{CHC} and pMOS^{DAHC}. Their E_a can explain ΔN_{it} recoveries and universality among the MOSFETs. Unfortunately, the origins of N_{ot} could not be determined; however, these findings shed light on HCS degradation and recovery mechanisms.

References

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Table I. Devices and HCS conditions in this study.

Sample	HCS condition	
	CHC(1000s, 298K)/abbreviation	DAHC1000s, 298K/abbreviation
pMOSFET	V_g=-4V, V_d=-4V/pMOS^{CHC}	V_g=-2V, V_d=-4V/pMOS^{DAHC}
nMOSFET	V_g=4V, V_d=4V/nMOS^{CHC}	V_g=2V, V_d=4V/nMOS^{DAHC}

Table II. Isothermal annealing and IAMEM experiments conditions

Experiment	Temperature scheme
Isochronal annealing (Fig. 1(a))	T_r= 373, 473, 573, 623K t_r=10, 30, 50, 100, 200, 400, 700, 1000, 2000, 4000, 7000, 10000, 12000, 14000, 15000, 18000s
IAMEM (Fig. 1(b))	T_a= 298-673K Δt=300s, ΔT=25K

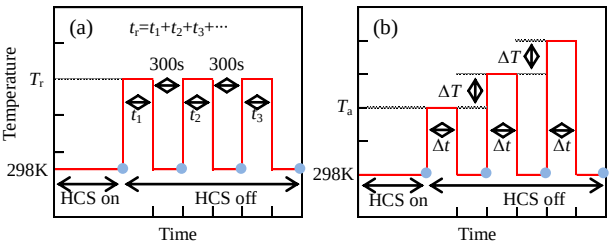

Fig. 1. (a): Isothermal annealing temperatures and (b): annealing temperatures for IAMEM experiments. Circles are ΔN_{it} measurements points.

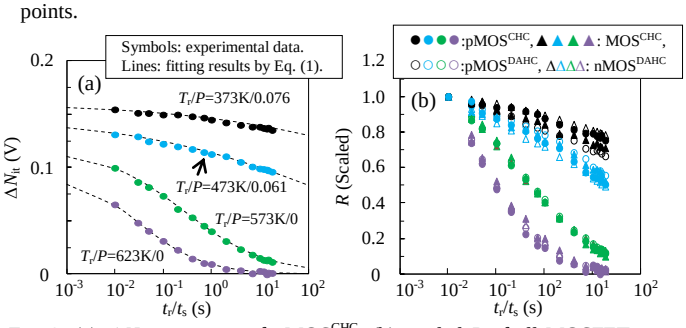

Fig. 2. (a): ΔN_{it} recoveries of pMOS^{CHC}. (b): scaled R of all MOSFETs.

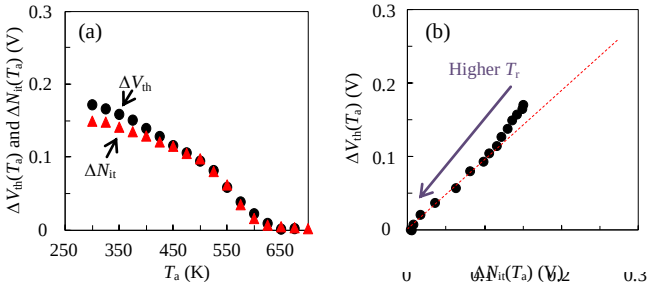

Fig. 3. (a): IAMEM experimental data of pMOS^{CHC}. (b): ΔV_{th} and ΔN_{it}. Dotted line is proportional line. For details, see text.

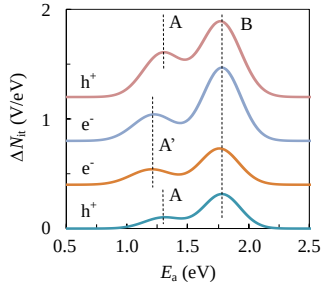

Fig. 4. IAMEM results (E_a). From bottom to top, pMOS^{CHC}, nMOS^{CHC}, pMOS^{DAHC}, and nMOS^{DAHC}. N_{ot} polarities are also depicted (h$^+$: hole, e$^-$: electron).

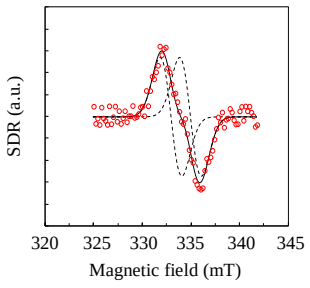

Fig. 5. SDR of pMOS^{CHC}. Circles are experimental data. Dotted and solid lines are P_b-center's line (Gaussian) and their summation, respectively.