

Fabrication of High Performance Single-Crystalline Silicon Thin Film Transistors on a Polyethylene Terephthalate Substrate

Kohei Sakaike¹, Muneki Akazawa¹, Akitoshi Nakagawa¹, and Seiichiro Higashi^{1,2}

¹ Department of Semiconductor Electronics and Integration Science,
Graduate School of Advanced Sciences of Matter, Hiroshima University,
Kagamiyama 1-3-1, Higashihiroshima, Hiroshima 739-8530, Japan
Phone: +81-82-424-7648 E-mail: semicon@hiroshima-u.ac.jp

² Research Institute for Nanodevice and Bio Systems, Hiroshima University,
Kagamiyama 1-4-2, Higashihiroshima, Hiroshima 739-8527, Japan

Abstract

A single-crystalline-silicon (c-Si) layer (supported by columns on a starting Si-on-insulator wafer) and a counter polyethylene terephthalate (PET) substrate were placed in close face-to-face contact, and pure water was sandwiched in between the c-Si layer and the PET substrate. The samples formed in this manner were heated on a hot plate at 80°C, and the SOI layer is transferred to PET by the meniscus forces. By applying the proposed transferred technique, high performance c-Si thin-film transistors (TFT) were successfully fabricated on the PET substrate, which showed a field-effect mobility as high as 552 cm² V⁻¹s⁻¹.

1. Introduction

Silicon CMOS technology is approaching the end of scaling due to unavoidable physical limitations. Still, we have to find out a new way to utilize its huge intellectual, human, and production resources. If single-crystalline Si (c-Si) thin-film-transistors (TFTs) were formed “locally at the required position” at a low temperature (150°C or less) on plastics, “flexible electronics” could be further advanced. Large-area electronics on the plastics substrate have been evolving on the basis of amorphous silicon, organic, and oxide semiconductor materials and low-temperature fabrication technologies such as solution-based process and printing technique. However, these devices such as TFT have serious problems originated from their low electrical performance, high operating voltage, and poor reliability under operation. In order to implement silicon technology on plastics substrates, device-transfer techniques employing exfoliation layers such as “surface-free technology by laser annealing” (SUFTLA) and “device-transfer technology by backside etching” (DTBE) have been reported [1, 2]. However, these techniques require complicated process and cannot solve high cost of production issues when applied to large area. In our previous work, a novel low-temperature technique for transferring a c-Si film by meniscus force has been proposed, and the c-Si film which formed in dog-bone shape (with size of 20 × 60 μm²) were successfully transferred to a polyethylene terephthalate (PET) substrate at its heatproof temperature or lower. [3,4] In this work, the transfer of smaller dog-bone shape c-Si to the PET sub-

strate by the proposed low-temperature layer transfer technique and fabrication of c-Si TFTs are investigated.

2. Experimental

The SOI layer [p-type Si(100), 10-30 Ω·cm] was patterned to form a 1-μm-wide and 4-μm-long dog-bone shape with 3×5-μm square regions at both ends, as shown in Fig. 1(a). This pattern is applicable to TFT fabrication to form a source, a channel, and a drain. To form supporting columns, holes with size of 1 × 1 μm were made at intervals of 1 μm in the square regions. As a result of this shape of Si film, the columns can be formed at both ends of the film, and the columns are suitable to form a stable midair-cavity. The buried-oxide (BOX) layer was etched by 33% hydrofluoric acid using the patterned SOI layer as a mask to form thin columns that support the SOI layer in air, as shown in Fig. 1(b). The starting and counter PET substrates were in close face-to-face contact with the filling water, and these substrates were heated on a hot plate at 80°C.

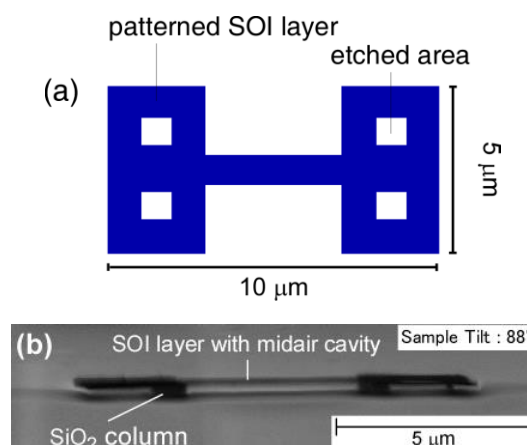


Fig. 1. (a) Plan-view schematic diagram of the SOI layer pattern used to form a stable midair-cavity. (b) Cross sectional SEM image of the midair SOI layer on a Si wafer.

Figure 2 schematically shows the meniscus force mediated layer transfer (MLT) of SOI layer to a foreign substrate.[3] As the water evaporates through the midair cavity,

capillary bridges are formed in between the SOI layer and the counter substrate and the meniscus force ($F = 2\pi R^2 \gamma \cos \theta_E / H$ ($H \ll R$)) rapidly increases with decreasing H (see Fig. 2 inset). Eventually, the SOI layer is transferred when removing the wafer.

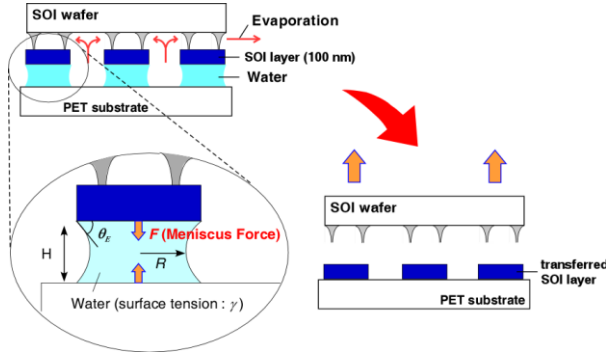


Fig. 2. Schematic illustration indicating the mechanism of transferring an a-Si film with a midair-cavity by meniscus force. Water initially filling the midair-cavity evaporates and attractive meniscus force transfers the Si film from the starting substrate to PET substrate.[3]

3. Results and Discussions

When the excessive water between the SOI wafer and counter PET substrate was evaporated, the original form and position of the SOI layer were completely maintained after the film transfer by separating these samples. Figure 3 shows the optical microscope images of SOI layer with midair cavity (which has size of $5 \times 10 \mu\text{m}^2$) on starting SOI wafer (a), and transferred Si films on PET substrate (b). These images confirm that a single-crystalline Si thin film was successfully formed on PET substrate at 80°C . In addition, multiple local transfers of a SOI layer from a SOI wafer were attempted by the proposed MLT technique. From this result, it is confirmed that the proposed MLT technique can locally and repeatedly transfer Si films to a pre-determined position.

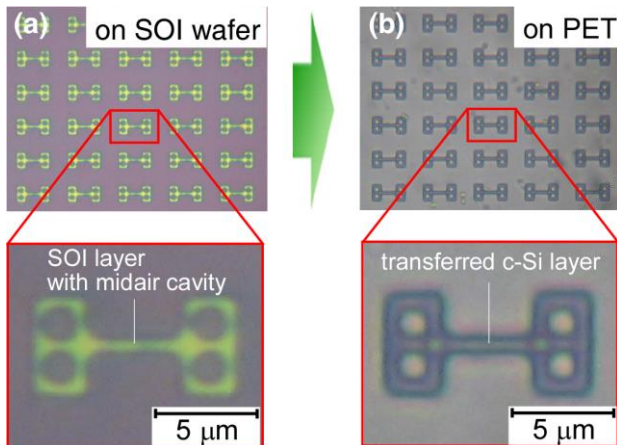


Fig. 3. Optical microscope images of (a) SOI layer with midair cavity (which has size of $5 \times 10 \mu\text{m}^2$) on starting SOI wafer, and (b) transferred Si films on PET substrate.

To confirm the adaptability of this layer transfer technique to thin-film devices, TFT were fabricated on a PET substrate. Here, the key process is the thermal oxidation and subsequent hydrogen anneal of the SOI layer on the midair cavity. This process ensures a good MOS interface, and the SiO_2 layer works as a “blocking” layer that blocks contamination from PET surface. [4] Figure 4 (a) shows I_d - V_g characteristics of the TFTs fabricated on a transferred c-Si film. The TFT dimensions are $L = 3.7 \mu\text{m}$ and $W = 3 \mu\text{m}$. The TFT showed a high field-effect mobility (μ_{FE}) of $552 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$.

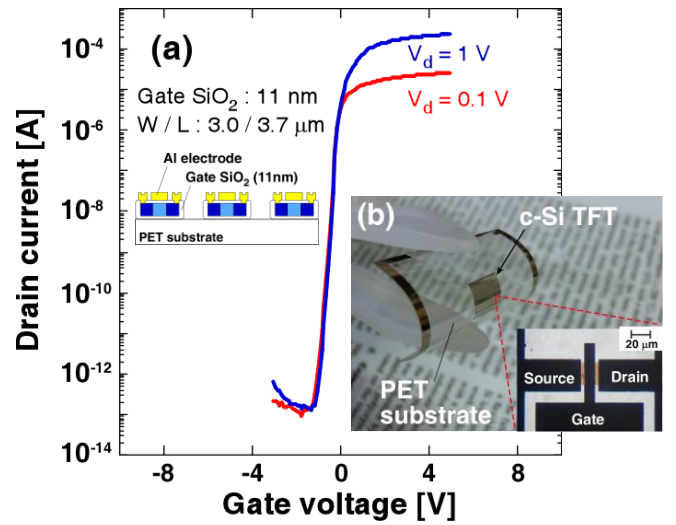


Fig. 4. (a) I_d - V_g characteristics of TFT on PET substrate, which has $L=3.7 \mu\text{m}$ and $W=3 \mu\text{m}$ fabricated with transferred Si films. (b) shows photographs of the flexible TFTs sheet and magnified transistor.

4. Conclusions

A c-Si layer supported by columns on a starting SOI wafer and a counter PET substrate were placed in close face-to-face contact, and pure water was sandwiched in between the c-Si layer and the PET substrate. By the meniscus forces generated during evaporation of the sandwiched water from the samples, the c-Si thin film was completely transferred to the PET substrate. High performance c-Si TFTs were successfully fabricated on the PET substrate, which showed a μ_{FE} of $552 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$.

Acknowledgements

This work is supported by Funding Program for Next Generation World-Leading Researchers (NEXT Program) and JSPS KAKENHI Grant Number 252156.

References

- [1] S. Inoue, et al.,: IEEE Trans. Electron Devices **49**, 1353 (2002).
- [2] S.-C. Wang,,et al., Jpn. J. Appl. Phys. **42**, L1044 (2003).
- [3] K. Sakaike et al., Jpn. J. Appl. Phys. **53**, 018004-1 (2014).
- [4] K. Sakaike et al., Appl. Phys. Lett, **103**, 233510-1 (2013).