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# Si-substrate-based High Mobility Ge-pMOSFETs Using Ozone Passivated $Al_2O_3/GeO_x$ Gate Dielectric

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**Abstract**

**By carefully control the Ge epitaxy process, high-k/Ge interface passivation, and junction formation, Si-substrate-based Ge-pMOSFETs with a peak mobility of 524 $cm^2/Vs$ and an $I_{on}/I_{off}$ ratio of $10^4$ is demonstrated and discussed. This work presents a good solution for high mobility pMOSFETs for future technology node.**

## 1. Introduction

Ge is a promising candidate to replace Si because of its high mobility. Towards the realization of high performance Ge-pMOSFET on Si, the main obstacles are: i) defects generated during Ge epitaxy on Si; ii) defects at the high-k/Ge interface. To deal with the former obstacle, defects density in the epitaxial Ge layer has been significantly reduced by selective growth of Ge in $SiO_2$ trenches and other methods [1]. While considering the high-k/Ge interface passivation, inserting a thin $GeO_2$ layer is regarded as one of the best solutions for a high-quality interface. Although $GeO_2$/Ge interface is generally considered to be thermodynamically unstable due to GeO desorption under high temperature [2], Lee et al. have applied high-pressure oxidation to suppress GeO desorption [3], while Zhang et al. have taken advantage of oxygen plasma and maintained an ultrathin $GeO_2$ interfacial layer at low temperature, and the $D_{it}$ value has been significantly reduced [4]. Ozone shows similar oxidation activity to oxygen plasma, making it become a possible way to for high quality $GeO_2$/Ge interface without causing GeO desorption. Albeit previous studies have made remarkable progress, the combination of Ge/Si integration and high mobility Ge-pMOSFETs fabrication still need further investigation. Therefore, it is quite meaningful to demonstrate more results about the integration of Ge-FETs with Si platform. In this paper, through the combination of a modified epitaxy method and ozone passivation technique, high mobility Ge-pMOSFETs integrated on Si platform is demonstrated and systematically characterized.

## 2. Experimental

Ge films were grown on n-Si (100) by RPCVD, through low temperature seed layer formation at 400°C followed by high temperature Ge layer growth at around 650°C. Fig. 1 shows the cross sectional TEM image of the epitaxial Ge/Si(100) substrate. Clearly, most defects are located in the low temperature seed layer while the high temperature layer contains almost no visible defects, indicating the formation of a high-quality epitaxial layer. This result is confirmed by high resolution-XRD. As depicted in Fig. 2, the width of Ge (004) diffraction peak is 190 arcsec, indicating that the epitaxial Ge layer is a well-arranged high quality film. Moreover, based on the results in Fig. 2, the epitaxial Ge layer is identified to be a fully relaxed one. After an HCl (12%) last cleaning process, the Ge/Si substrates were transferred to the ALD system. Then the first 0.3nm $Al_2O_3$ as oxygen blocking layer was deposited onto the Ge/Si substrate at 300°C. Ozone oxidation was *in situ* performed at 300°C to build $Al_2O_3/GeO_x$/Ge stack. The $GeO_x$ thickness is estimated to be 0.6nm by ellipsometry. Then, additional 4.8nm $Al_2O_3$ was deposited, followed by annealing in 1atm $O_2$ at 550°C for 10min. For the Si-based Ge-pMOSFETs, P was firstly implanted to form an n-well, and then the wafers were annealed in $N_2$ at 650°C for 30min to reach a unified doping level ($3x10^{16}cm^{-3}$). After that, $Al_2O_3/GeO_x$ stack formation was performed using the above process. Ti/Au gate electrode was deposited and patterned after the gate stack formation. Then, the source/drain regions were formed by B+ implantation, followed by activation annealing. The Ni/Pt/Au source/drain contacts were deposited by evaporation. At last, C-V and I-V characterizations were performed.

## 3. Results and discussion

Fig. 3 shows the C-V characteristics of the $Al_2O_3/GeO_x$/Ge/Si stack. The EOT extracted from the accumulation region is about 2.5nm. Well behaved C-V curves with small frequency dispersion indicate the $D_{it}$ at the interface is quite low. Inset shows the $D_{it}$ distribution in the upper half gap of Ge for this stack extracted by conductance method. Compare with the gate-stack without $GeO_2$ and the one with $GeO_2$ but formed by thermal oxidation, the ozone passivated stack shows a lower $D_{it}$ value about $<5x10^{11}cm^{-2}eV^{-1}$, and becomes identical from $E_i$+0.1eV~0.2eV. Fig. 4(a) and (b) show the $I_d$-$V_g$ and $I_d$-$V_d$ characteristics of the Si-substrate-based Ge-pMOSFET with channel size of 400μm/24μm (W/L). The threshold voltage is fitted to be -0.2V, indicating the device works in the enhancement mode. Moreover, the drain current $I_{on}/I_{off}$ ratio is found to be over $10^4$ with a SS factor of 105mV/dec. To further illustrate the advantage of ozone passivation, the $I_{on}/I_{off}$ ratio against interface passivation is compared by

using Ge-pMOSFETs. As shown in Fig. 5(a), higher $I_{on}/I_{off}$ ratio is obtained from the Ge-pMOSFET using ozone oxidation than the ones with thermal oxidation and the ones without $GeO_2$ formation. Since off-state current is mainly determined by the junction quality, thus the $I_{on}/I_{off}$ ratio against junction formation is also studied using Si-based Ge-pMOSFETs. As depicted in Fig. 5(b), compared with the pFET without n-well formation and the one with n-well formation but deeper junction, the one with n-well formation and shallower junction demonstrates larger $I_{on}/I_{off}$ ratio. Thanks to the n-well formation and S/D junction optimization, this $I_{on}/I_{off}$ ratio almost catches up with that of our p-MOSFETs using pure Ge substrate. To extract the effective hole mobility of the fabricated pMOSFETs, split C-V method was used. Fig. 6 shows the split C-V characteristics of the pMOSFETs with various frequencies, the nearly dispersion-free curves indicate excellent interface quality with low $D_{it}$ value. Fig. 7 shows the effective hole mobility of the Si-substrate-based Ge-pMOSFET, a peak mobility at $N_s=3x10^{11}cm^{-2}$ is extracted to be 524 $cm^2/Vs$ after $R_s$ correction. Compare with Si universal mobility, the fabricated Si-substrate-based Ge-pMOSFETs shows 3.5x mobility enhancement, suggesting that Ge-pMOSFETs integrated on Si platform is a prospective solution for future high performance devices.

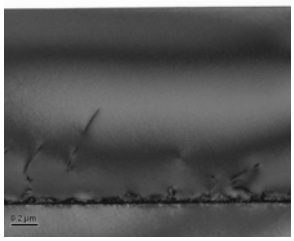

Fig. 1 Cross sectional TEM image of the epitaxial Ge on Si (100).

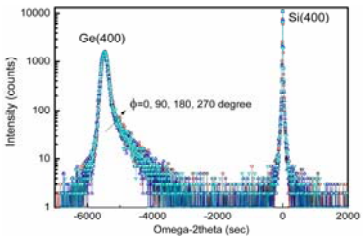


Fig. 2 High resolution-XRD spectra with in-plane rotation angle (ϕ) of 0, 90, 180, and 270 degree.

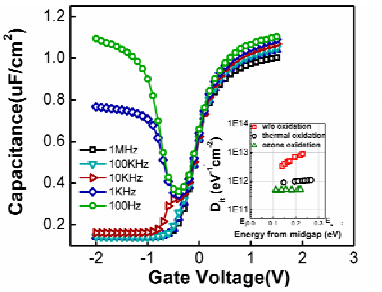


Fig. 3 C-V curves of $Al_2O_3/GeO_x/Ge/Si$ stack. Inset shows the $D_{it}$ distribution @Ei+0.1eV~0.2eV.

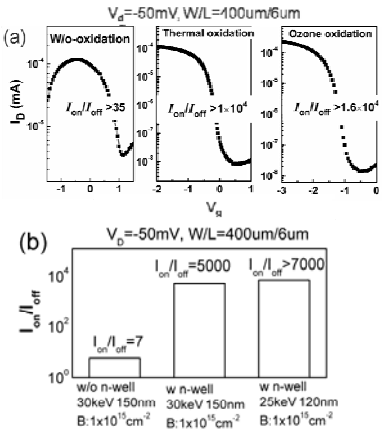


Fig. 5 Comparison of $I_{on}/I_{off}$ ratio against (a) interface passivation using Ge-pMOSFETs and (b) n-well formation and junction depth using Si-based Ge- pMOSFETs.

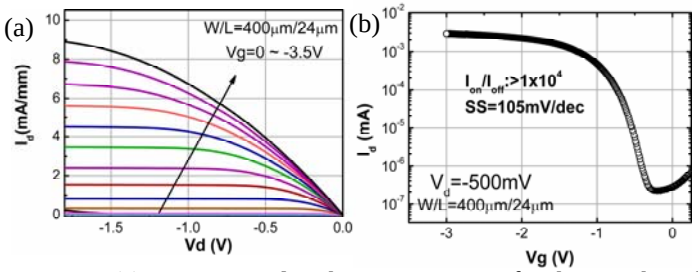


Fig. 4(a) $I_d$-$V_g$ and characteristics of the Si-based Ge-pMOSFETs with $V_d$=-500mV. $I_{on}/I_{off}>10^4$, SS=105mV/dec. (b) $I_d$-$V_d$ characteristics of the Si-based Ge-pMOSFETs

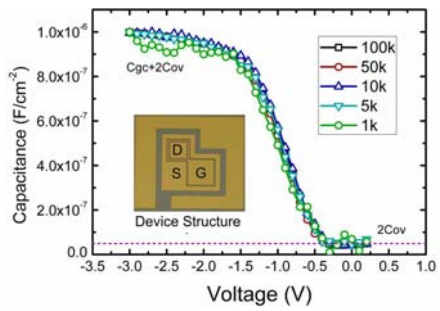


Fig. 6 The split C-V curves for the p-MOSFETs, where the inset shows the device structure. Small frequency dispersion indicates a low $D_{it}$ value.

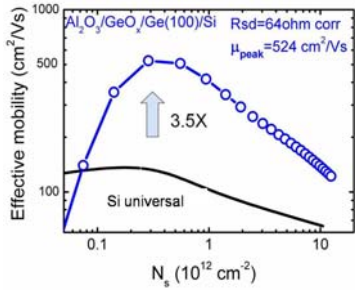


Fig. 7 Effective hole mobility of the Si-based Ge-pFETs, the peak mobility is estimated to be 524 $cm^2/Vs$ after $R_s$ correction

## 4. Conclusions

A two-step epitaxy method is successfully introduced into the hetero-integration process of Ge with Si platform. By taking good care of high-k/Ge interface using ozone treatment, high-quality $Al_2O_3/GeO_x/Ge/Si$ gate stack with nearly dispersion-free C-V characteristics and low $D_{it}$ value is obtained. Based on this stack, Si-substrate-based Ge-pMOSFETs with a peak mobility of 524 $cm^2/Vs$ and an $I_{on}/I_{off}$ ratio of $10^4$ are obtained, which gives a strong evidence for integrating Ge on Si platform for p-MOS application in advanced technique node.


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