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Flexible Silicon-Germanium Devices With High-k/Metal Gate Stacks For Next Generation High Hole Mobility Channel Devices

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Abstract

Silicon germanium (SiGe) has received considerable attention as an alternate channel material to replace silicon as next generation high-hole mobility channel devices (specifically for p-MOSFETs). We demonstrate in this work a CMOS compatible cost-effective process to transform epitaxially grown silicon-germanium based arrays of high-k/metal gate based metal oxide semiconductor capacitors (MOSCAPs) into flexible and semi-transparent one. We show outstanding mechanical flexibility (bending radius of 4 mm), and optical semi-transparency of 6%, with good electrical characteristics assessed under mechanical bending conditions.

1. Introduction

Silicon-germanium (SiGe) has gathered attention over conventional silicon, especially in p-channel devices, due its intrinsic higher hole mobility [1] and silicon manufacturing compatibility. SiGe technology has enabled key advancements in silicon based microelectronics technology, such as the development of hetero-junction bipolar transistors (HBTs) for radio-frequency (RF) communications [2], and strained metal-oxide-semiconductor field-effect transistors (MOSFETs) for high performance nanoelectronics [3, 4], enabling not only high speed computation, but also low power energy-efficient electronics for a more sustainable future. As a promise for lightweight, low-cost, and multifunctional devices, flexible electronics on strained SiGe platform have been demonstrated through the transfer-printing technique, however the technique is not suitable for expansion to the state-of-the-art complementary metal oxide semiconductor (CMOS) technology due to its low integration density and high expense [5, 6]. Therefore, in this work we report transformation of high-k/metal gate based devices fabricated on epitaxially grown SiGe on bulk mono-crystalline silicon (100) into flexible and semi-transparent one while maintaining device performance, integration density, cost and reliability [7, 8].

2. Fabrication Process

First, 400 nm of $Si_{0.58}Ge_{0.42}$ epitaxy film was grown on a standard lightly doped p-type bulk mono-crystalline (100) wafer, through a low pressure chemical vapor deposition technique (LPCVD), which was assisted by a ~25 nm epitaxially grown Si buffer layer [Fig. 1(a)]. Surface roughness of ~ 12 nm [Fig. 1(b)], 42% Ge composition [Fig. 1(c)], and 2% compressive strain [Fig. 1(d)], were respectively determined through atomic force microscopy (AFM), Raman analysis and X-ray diffraction analysis. Then, MOSCAP fabrication was carried out through silicon oxide (SiO_2) patterning for isolation, deposition of high-k/metal gate stack with 10 nm aluminum oxide (Al_2O_3) and 20 nm tantalum nitride (TaN), and sputtering of aluminum (Al) contacts, as shown in Fig. 2(a) and (b). To release the devices, etch holes were opened up, through which SiGe/Si fabric is etched away to create deep trenches in the substrate. After protecting the sidewalls of the trenches with Al_2O_3 spacers, we release the top portion of our wafer by exposing the devices to a xenon difluoride ($XeFe_2$) isotropic etchant. This allows the formation of caves around the trenches [Fig. 2(c)], which eventually merge and detach the top portion of the substrate with the fabricated SiGe devices on top.

3. Results and Discussion

We release 10 μm thick of SiGe/Si fabric, with the already fabricated MOS capacitors. The released sample (10 μm x 3 μm x 1.5 μm) shows optical semi-transparency of ~6% in the visible range [Fig. 3(a) and (b)], and mechanical flexibility with minimum bending radius of 0.4 cm [Fig. 3(c)]. Capacitance-voltage (C-V) and current density (J-V) characteristics were performed before and after release, and under concave mechanical bending setup [Fig. 4], showing a normalized capacitance value of ~0.7 $\mu F/cm^2$ and a leakage current density of ~0.5 mA/cm^2 at a bias voltage of -1V after devices are released [Figs. 4(a–d)]. Bending did cause further discrepancy in leakage current [Fig. 4(e)], nevertheless the results achieved for the flexible p-type $Si_{0.58}Ge_{0.42}$ MOS capacitors are very comparable to capacitance values found in the literature for p-type SiGe based MOSCAPs with high-k Al_2O_3 dielectric [9, 10]. Degradation of leakage current involves micro to nano-scale cracking in dielectric related to bending.

4. Conclusion

We demonstrate the first successful transfer-less release of SiGe high-k/metal gate MOS capacitors on flexible platform, using state-of-the-art cost-effective CMOS compatible processes, a pragmatic step towards truly high-speed low-cost flexible systems.

References:

[1] S. Iyer *et al.*, *IEEE Electron Device Letters*, **12** (1991) 5; [2] B. Heinemann *et al.*, *Electron Devices Meeting (IEDM)*, (2010) 30.5.1; [3] D. J. Paul, *Advanced Materials* **11**, (1999) 3; [4] J-Y Wei *et al.*, *Solid-state electronics*, **50** (2006) 2; [5] H. Zhou *et al.*, *Scientific reports* **3** (2013); [6] H. Yuan *et al.*, *Semiconductor science and technology* **22** (2007) 1; [7] J. P. Rojas *et al.*, *IEEE transactions on electron devices* **60** (2013) 10; [8] G. T. Sevilla *et al.*, *Advanced Materials* **26** (2014) 15; [9] F. Bellenger *et al.*, *ECS Transactions* **16** (2008) 5; [10] J. Han *et al.*, *presented at the Group IV Photonics (GFP) for IEEE 9th International Conference*, (2012) 144.

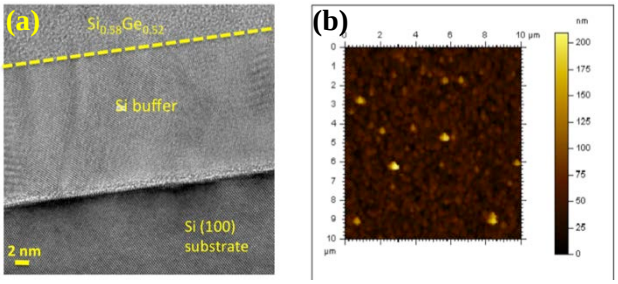

FIG. 1 (a) Transmission electron microscopy (TEM) image showing monocrystalline structure of Si epitaxial buffer and epitaxial $Si_{0.58}Ge_{42}$ film; (b) Epitaxial SiGe film with 42% Ge content [S_q= 18.1 nm; S_a= 12.4 nm].

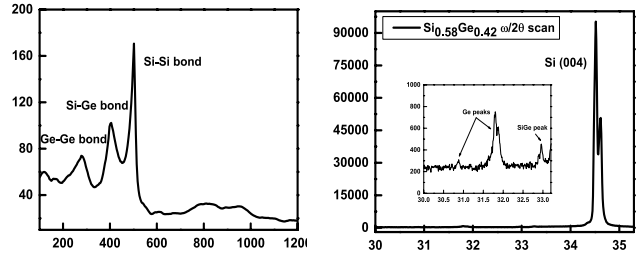

FIG. 1(c) Raman analysis of $Si_{0.58}Ge_{0.42}$ alloy. Si-Ge bond appears at 405.55 $cm^{-}1$, Si-Si bond at 502.4 cm^{-1}, and Ge-Ge bond at 277.6 cm^{-1}. (d) Omega/2theta XRD scan, with SiGe peak at θ=32.95°, Si peak at θ=34.52°, and Ge peak at θ=30.87°.

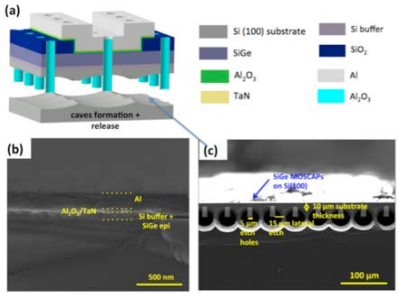

FIG. 2 (a) Schematic of final device structure after release; b) SEM image of the MOSCAPs gate stack; c) SEM image showing formation of caves before total release of the top portion.

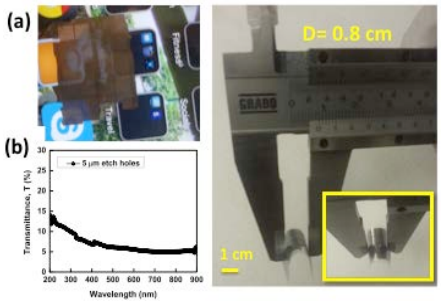

FIG. 3 (a) Digital photo showing semi-transparency of the sample on mobile background; (b) Transmittance spectrum of released SiGe devices; (c) Bending radius showing outstanding flexibility of sample.

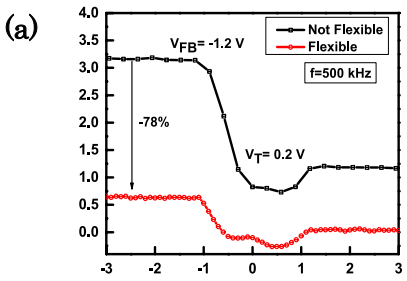

FIG. 4(a) C-V characteristics of $Si_{0.58}Ge_{0.42}$ MOSCAPs before and after flexible at 500 kHz, exhibiting a 78% decrease in capacitance after release.

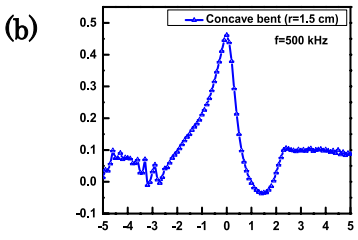

FIG. 4(b) C-V characteristics of $Si_{0.58}Ge_{0.42}$ MOSCAPs at 500 kHz, under tensile bent condition.

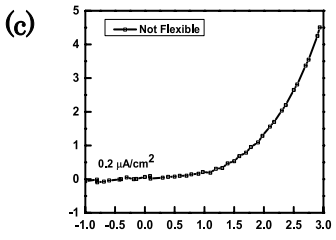

FIG. 4(c) J-V characteristics of $Si_{0.58}Ge_{0.42}$ MOSCAPs before flexible, displaying extremely low leakage current density at -1V bias voltage.

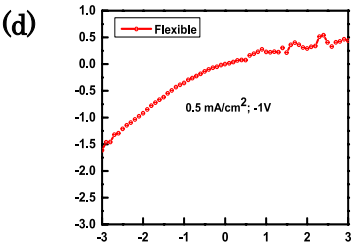

FIG. 4(d) J-V characteristics of $Si_{00.58}Ge_{0.42}$ MOSCAPs after release, showing an increase in leakage current at -1V by nearly three orders of magnitude.

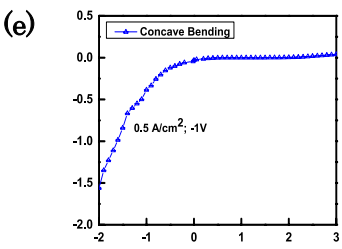

FIG. 4(e) J-V characteristics of $Si_{0.58}Ge_{0.42}$ MOSCAPs under bent conditions, exhibiting further increase in leakage current at -1V by an additional three orders of magnitude.