Transformation of Holes Emission paths under Negative Bias Temperature Stress in deeply scaled pMOSFETs

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Abstract

In this paper, the impact of negative bias temperature (NBT) stress on the \( I_G \)-RTN and \( I_D \)-RTN was studied for deeply scaled pMOSFETs. It is observed that low NBT stress only results in \( I_D \)-RTN while high NBT stress triggers additional \( I_G \)-RTN. By the analysis of the field dependence of emission constant, it is found that under low NBT stress, the stress generated traps exchange holes with the channel while under high NBT stress, at least some of traps discharge holes to the gate side.

1. Introduction

Recently, Random Telegraph Noise (RTN) signal has been observed in negative bias temperature instability. The simultaneously observation of \( I_G \)-RTN and \( I_D \)-RTN under NBT stress has been reported. As the time constants and amplitudes of these RTN are almost the same, it is suggested both share the same physical origin [1-2]. However, by now, the physics mechanism of \( I_G \)-RTN is still an issue [3-4]. In this paper, we studied the impact of NBT stress on \( I_D \)-RTN and \( I_G \)-RTN for deeply scaled pMOSFETs. The carrier separation measurement was used to determine the main carriers in \( I_G \)-RTN and the field behavior of RTN was investigated to identify the physical process of carrier transport under various NBT stress.

2. Various RTN behaviors under NBT stress

The experiments were carried out on pMOSFETs with 45nm technology nodes. Fig.1(a) and (b) show the time traces of \( I_G \) and \( I_D \) monitored simultaneously under the relative low (\( V_G = -1.3 \) V, \( E_{ox} = 3.1 \) MV/cm) and high (\( V_G = -2.1 \) V, \( E_{ox} = 6.2 \) MV/cm) stress. \( I_D \)-RTN is clearly detected in both stress conditions. On the other hand, only the high stress voltage in Fig.1(b) triggers \( I_G \)-RTN. The strong correlation between \( I_G \)-RTN and \( I_D \)-RTN suggests that they share the same origins.

Fig. 2 shows the field dependence of capture time (\( \tau_c \)) and emission time (\( \tau_e \)) for \( I_D \)-RTN within the gate voltage range of (-1.0 V~1.3 V) and (-1.8 V~2.1 V). For the low stress range, \( \tau_c \) and \( \tau_e \) are found to exponentially decrease and increase with \( V_G \) respectively, which can be explained by the extended non-radiative multi-phonon (eNMP) theory [5]. In this theory, when the negative gate bias is applied for pMOSFETs, the switching trap states can be created from Si-Si precursors in the oxide state by capturing a hole via a multi-phonon emission (MPE) process. The increase of the gate field results in a lower MPE barrier. The latter enhances the charge transfer reaction, leading to the dramatically reduction of hole capture time and the increase of hole emission time. However, eNMP theory is difficult to explain the electrical behavior of \( \tau_e \) in the stress range of (-1.8 V~ -2.1 V) where it keeps weakly dependent with the field. The unusual electrical behavior of \( \tau_e \) in the high stress range could be due to that the hole emission from the generated NBTI-induced switching trap is not to the Si substrate side but to the gate side. Microscopically, when the large \( V_G \) is applied, the tunneling probability of trapped carrier to the gate electrode side becomes larger. If this tunnel path is constructed, the gate leakage should increase and \( I_G \) current should decrease, which is consistent with the results observed in Fig.1(b).

3. Hole emission from traps to gate side

To obtain better insight into the emission process, we first use the carrier separation measurement to identify the major carriers involved in \( I_G \)-RTN. As shown in Fig. 3, \( \Delta I_G \) and \( \Delta I_{hhol} \) show the all same discrete fluctuation in the time traces, informing that the major carriers in \( I_G \)-RTN are holes. We then measure the field and temperature dependence of \( I_G \)-RTN amplitude under the relative high stress. As shown in Fig. 4, \( I_G \) increases with the stress voltage \( V_G \). Besides, extremely weak temperature dependence of \( I_G \) is observed in the inset of Fig.4, which is the typical behavior of the tunneling leakage process. To quantitatively indentify the bias dependence of \( I_G \)-RTN amplitude, a one step TAT model is constructed based on the hole tunneling via NBTI-induced switching traps. The model is described in Table 1. Fig.4 shows the experimental and simulated \( \Delta I_G \), the simulated data has a good agreement with the experimental data, demonstrating that the stress generated switching trap could assist hole tunneling.

Besides \( I_D \)-RTN and \( I_G \)-RTN, the step-like fluctuations are also detected in \( I_D \) current in Fig. 1(b). Fig. 5 shows the transformation of \( I_D \)-Step to \( I_D \)-RTN when the stress bias decreases from -1.7 V to -1.2 V. The results inform that these step-like fluctuations have the same physical origins of \( I_D \)-RTN detected under the low gate bias range in Fig. 1(a) and they can be considered as \( I_D \)-RTN with very long emission time \( \tau_e \) in the meaning that the holes are captured by the traps but they are difficult to be emitted.

Based on the above results, the charge trapping and detrapping process under various NBT conditions are illustrated in Fig. 6. Under the relative low gate stress, the generated switching traps capture and emit holes with the channel. Under the high gate stress, some holes are captured by the traps and emitted from the trap centers to the gate side while others are located in the trap center with
a quite long time.

4. Conclusions

The impacts of negative bias temperature (NBT) stress on the $I_{G}$-RTN and $I_{D}$-RTN were studied for deeply scaled pMOSFETs. It is observed that the low NBT stress only results in $I_{G}$-RTN while high NBT stress riggers additional $I_{D}$-RTN. By investigating the field dependence of RTN, the transformation of holes emission paths under NBT stress are identified.

![Fig. 1 The time trace of $I_{G}$ and $I_{D}$ fluctuation under the gate voltage $V_{G}$ of -1.3 V and -1.9 V with $V_{D}$ of 50mV.](image)

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![Fig. 2 Field dependence of $\tau_{e}$ and $\tau_{c}$ of the RTN under (a) higher and (b) lower gate bias regions. The red lines present MPFAT simulation results for $\tau_{c}$.](image)

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![Fig. 3 The time traces of gate current, electron current and hole current under NBT stress (-1.9 V) at $T$=320 K by using carrier separation technique.](image)

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![Fig. 4 The field dependence of $\Delta I_{G}$ amplitude. The red dash line presents the simulation results by trap-assisted tunneling (TAT) modeling. The inset shows temperature behaviors of $\Delta I_{G}$.](image)

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![Fig. 5 The transformation of transience signal from $I_{D}$-Step to $I_{G}$-RTN could be seen by decreasing the gate bias from -1.7 V to -1.2 V.](image)

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![Fig. 6 Schematic view of transformation of holes emission paths. Under low stress, the switching traps capture and emit holes with the channel. Under high stress, some holes are captured by the traps and emitted from the trap center to the gate side while others are located in the trap center with a long emission time.](image)

Fig. 6 Schematic view of transformation of holes emission paths. Under low stress, the switching traps capture and emit holes with the channel. Under high stress, some holes are captured by the traps and emitted from the trap center to the gate side while others are located in the trap center with a long emission time.

| Table I. The trap induced gate leakage obtained by TAT model [6] |

$I_{TAT} = A F_{OX}^{2} \cdot \left( \frac{\phi_{T}}{x F_{OX}} \right) \cdot \left( \frac{2 \phi_{T}}{x F_{OX}} - 1 \right) \cdot \exp \left( - \frac{8 \pi \sqrt{2m_{ox} \phi_{T}^{3}}}{3h q F_{OX}} \left[ 1 - \left( 1 - \frac{x F_{OX}^{3}}{\phi_{T}} \right)^{3} \right] \right)$ (1)

Here $\phi_{T}$ is the energy depth of the trap from the valence band of dielectric, $m_{ox}$ is the hole effective mass in dielectric, $F_{OX}$ is electric field in oxide and $x$ is the trap’s distance from the interface of gate and oxide. When $x = 1.5$ nm, and $\phi_{T} = 4$ V, it is observed that it provides a good description of the experimental data in fig. 4.

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References