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Assessment of Self Heating Effect (SHE) on Negative Bias Temperature Instability in SOI FinFETs under Circuit Operation

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Abstract

This paper investigated the impact of SHE on NBTI degradation at 16nm SOI FinFETs by 3D TCAD simulations. The SHE causes about 11.7% of I_{ds} degradation and aggravates NBTI degradation severely. The modified NBTI model with SHE is proposed and verified under various stress conditions.

1. Introduction

FinFETs are regarded as the most promising candidate for scaling down due to their excellent electrostatic integrity [1]. However, heat dissipation in such nano-scale structures with narrow fins and buried oxide presents significant challenges for device optimization and circuit design [2]. Although many works [3-5] have been reported to investigate the self-heating effect (SHE) experimentally and theoretically, only few works assesse the influences of SHE, especially on reliability issues. In this work, 3D TCAD simulations are performed to explore the impact of SHE on negative bias temperature instability (NBTI) in 16nm SOI FinFETs under circuit operation. The modified NBTI model is proposed and verified under various circuit operation conditions.

2. Device structure and simulation method

The simulated SOI FinFETs structure is illustrated in **Fig. 1(a)** with parameters listed in **Table I**. The structure and electrical parameters of SOI FinFETs in the simulations are designed with reference to the 2013 ITRS requirements for high performance logic device at 16nm technology node [6]. 3D hydrodynamic transport model and density gradient quantum correlations self-consistent with lattice temperature equation are employed to investigate SHE by Sentaurus [7]. The boundary thermal conductance [8] are applied to the contacts shown in **Fig. 1(b)**. Our simulation is calibrated with experiments of 90nm p-channel SOI FinFETs [9], as shown in **Fig. 2**. The two-stage NBTI degradation model [10] coupled with the transport model and lattice temperature equation are employed to assess the impact of SHE on NBTI degradation. Considering the accuracy of this NBTI model in long stress duration [11], the simulation stress times range from 1μs to 1s.

3. Results and discussion

Fig. 3(a) illustrates the temperature distribution in the 16nm SOI FinFETs at saturation condition. The peak temperature is over 410K located in drain extension. The I_{ds}-V_{ds} with/without SHE is shown in **Fig. 3(b)**. The I_{ds} degradation caused by SHE at V_{gs}=V_{ds}=-0.86V is 11.7%. This indicates that SHE can't be ignored in 16nm SOI FinFETs. The thermal resistances (R_{th}) in SOI FinFETs are extracted in **Fig. 4**. The statistical average temperature in silicon under various total power for SOI FinFETs with gate length is shown in **Fig. 4(a)**. The slope of average temperature with respect to total power is the extracted R_{th} shown in **Fig 4(b)**. With the gate length scaling down, the R_{th} increases and SHE becomes severer.

In order to investigate the impact of SHE on NBTI reliability during circuit operation. Gate voltage stress ($V_{gstress}$) with a small drain bias (V_{ds}) [12] was applied. The lattice temperature distribution along the channel with different stress condition is shown in **Fig. 5**. The temperatures are not uniform along the channel and increase with $V_{gstress}$ at a constant V_{ds} or V_{ds} at a constant $V_{gstress}$. The NBTI degradation simulation results with different stress conditions are shown in **Fig. 7** and **Fig. 8**. **Fig. 7** shows the V_t shift with respect to stress time at different $V_{gstress}$ with a small V_{ds} bias (V_{ds}=-0.5V) with/without SHE. The results show that the SHE aggravates about 50% of NBTI degradation at $V_{gstress}$=-1.5V V_{ds}=-0.5V. **Fig. 8** shows the V_t shift with stress time at different V_{ds} bias with a constant $V_{gstress}$=-1.0V with/without SHE. The degradation without SHE decreases with increasing V_{ds} bias because large V_{ds} decreases E_{ox}. However, when takes the SHE into consideration, the degradation increases with increasing V_{ds} bias due to that large V_{ds} causes high channel temperature based on **Fig. 5**.

Considering the impact of SHE on NBTI, the temperature ($T_{ambient}$) in conventional model should be modified. Therefore, lattice temperature ($T_{lattice}$) is used to represent $T_{ambient}$ shown in **Fig. 6**. Based on the modified model, the NBTI simulation at $T_{lattice}$ without SHE (line) is consistent with the simulation with SHE at $T_{ambient}$ (open symbol) shown in **Fig. 7** and **Fig. 8**.Those indicate that the modified model is valid for NBTI with the impact of SHE.

4. Conclusions

A 3D TCAD simulation is used to assess the impact of SHE on NBTI degradation at 16nm SOI FinFETs. The SHE leads to 11.7% of I_{ds} degradation at saturation condition and the temperature distribution along channel is not uniform. The NBTI degradation with SHE increases with increasing $V_{gstress}$ at a constant V_{ds} or increasing V_{ds} at a constant $V_{gstress}$. The SHE aggravates about 50% of NBTI degradation at $V_{gstress}$=-1.5V V_{ds}=-0.5V compared with the NBTI degradation without SHE. The modified NBTI model with SHE is proposed and verified under various stress conditions.

Acknowledgements

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References

[1] J.P Colinge, 2008 Springer. [2] T. Takahashi, et al., Jpn. J. Appl. Phys. **52** (2013). [3] K. Kukita, et al., *IEDM*, 2012 411-414.

[4] A. Wang, *SSDM*, 2013, 86-87. [5] S. Makovejev., et al., TED **60** (2013). [6] ITRS, 2013 http://www.itrs.net/. [7] Sentaurus TCAD User Manual, Synopsys, Inc., V2012.06. [8] S. Kolluri, et al., *IEDM*, 2007 177-180. [9] N. Xu, et al., *IEDM*, 2010 194-197. [10] T. Grasser, et al., *IRPS*, 2009 33-44. [11] S. Gupta, et al., *IRPS*, 2012 XT.3.1-3.6. [12] U. Monga, et al., EDL **33** (2012)

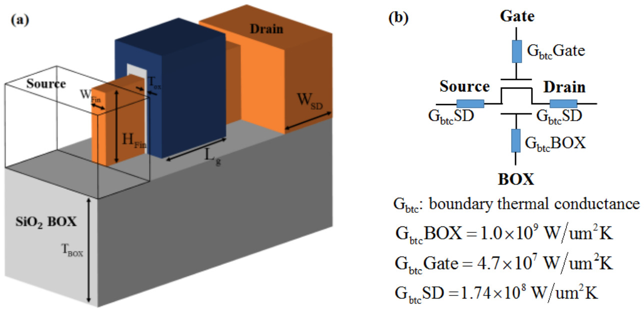

Fig. 1(a) The device structure and **Fig. 1(b)** The boundary thermal conductance in the TCAD SHE and NBTI simulation.

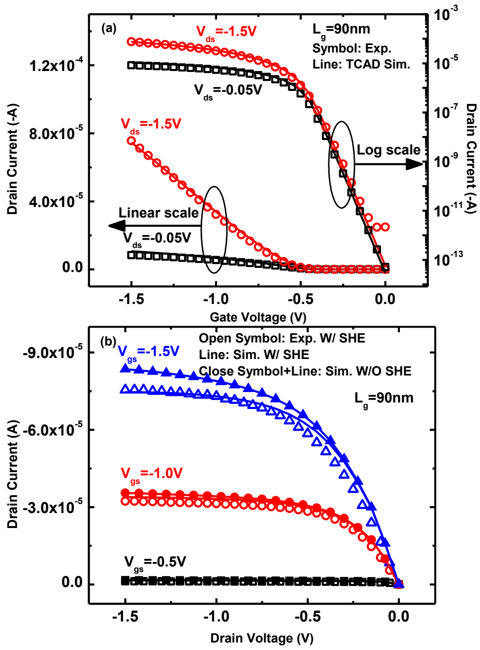

Fig. 2(a) (b) TCAD calibration with 90nm SOI FinFETs experiments, showing the validity of the simulation methods.

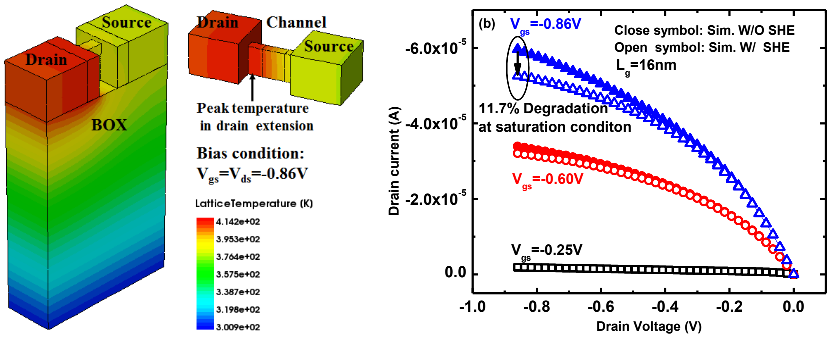

Fig. 3(a) The temperature distribution in the 16nm SOI FinFETs. The peak temperature is above 410 K and locates in drain extension at saturation operation. **Fig. 3(b)** The I_{ds}-V_{ds} characteristics with/without SHE. The I_{ds} degradation caused by SHE at V_{gs}=V_{ds}=-0.86V is 11.7%.

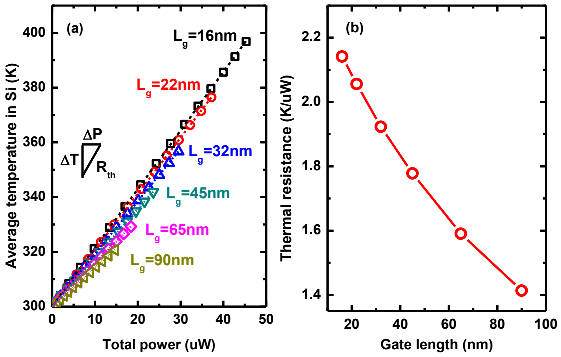

Fig. 4(a) The average temperature in silicon under various total power for SOI FinFETs with different gate length. **Fig. 4(b)** The extracted thermal resistance with different gate length.

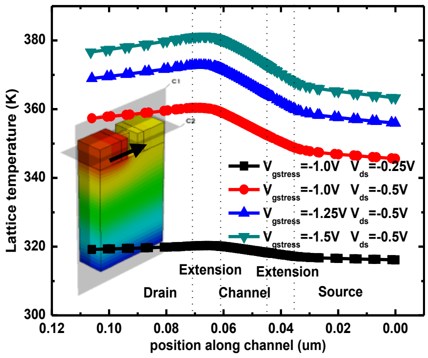

Fig. 5 The lattice temperature distribution along the channel (cross line of plane C1 and C2) at different stress conditions.

NBTI model[10]

$$Q = Q_{ox} + Q_{it} = qN_0 < s_2 + s_4 > + qN_0 < s_4 f_{it}^p >$$

$$\Delta V_t = \frac{Q}{C_{ox}} = \frac{Q_{ox} + Q_{it}}{C_{ox}}$$

NBTI W/O SHE:

$$\Delta V_t = A(E_{ox}, T_{ambient}) \times t^n$$

Modified NBTI W/ SHE:

$$\Delta V_t = A(E_{ox}^{'}, T_{Lattice}) \times t^n$$
$$= A(E_{ox}^{'}, T_{ambient} + I_{ds} V_{ds} R_{th}) \times t^n$$

Fig. 6 The two-stage NBTI model and modified NBTI model used in our simulation.

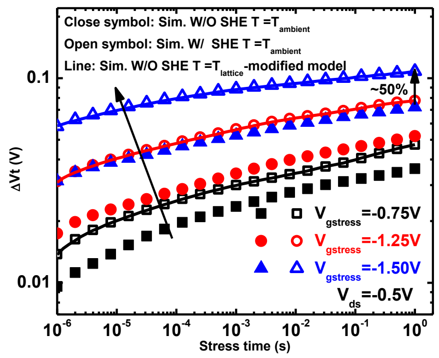

Fig. 7 The V_t shift with stress time at different $V_{gstress}$ with a small V_{ds} bias with /without SHE. It shows that SHE aggravates NBTI degradation seriously and the modified NBTI model is validity for NBTI with the impact of SHE.

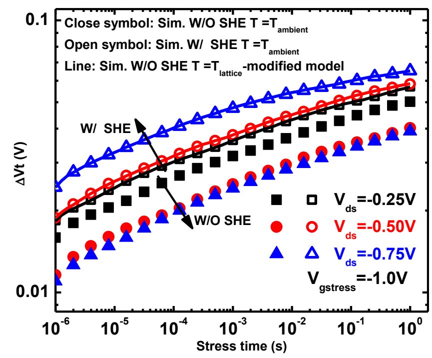

Fig. 8 The V_t shift with stress time at different V_{ds} bias with constant $V_{gstress}$=-1.0V. It shows that V_t shift decreases with increasing V_{ds} without SHE because large V_{ds} decreases E_{ox}. V_t shift increases with increasing V_{ds} with SHE because large V_{ds} leads to high temperature.

Table I Parameters used in this study

PARAMETER	VALUE
Gate Length (L_g)	16 nm
Fin Height (H_{Fin})	20 nm
Fin Width (W_{Fin})	6.4 nm
Side Dielectric Thickness (T_{ox})	0.8 nm
Top Oxide Thickness	>5 nm
BOX(T_{BOX})	150 nm
Channel Doping (N_{ch})	1×10^{15}cm^{-3}
S/D Doping ($N_{S/D}$)	3×10^{20}cm^{-3}
The precursor density in NBTI simulation (N_0)	5×10^{12}cm^{-2}