Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials, Tsukuba, 2014, pp22-23

The impact of positive bias temperature instabilities on stacked high-k/metal gate transistor with TiN barrier layer

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1. Introduction

In more recent years, high-k/metal gate (HK/MG) has been attractive for high-speed and low-power logic metal–oxide–semiconductor field-effect transistor (MOSFET) applications. However, positive bias temperature instability (PBTI) has been recognized as a major reliability issues in advanced systems containing HK/MG dielectrics. The impact of traps on the PBTI behaviors in high-k dielectric has been extensively studied [1-2]. Oxygen and nitrogen vacancies are known to play an important role in the threshold voltage instability as a result of the oxide trapped charges and interface traps in metal-gate/HfO_2/SiO_2 structures during thermal treatment [3]. Previous studies have demonstrated that defects can be reduced in high-k dielectrics by post metallization annealing (PMA) without increasing the oxide thickness [4-5]. This annealing process is used to reduce the oxygen vacancy by incorporating the oxygen to suppress the threshold voltage instability. In this paper, the correlation between device reliability and performance in the PMA process with various TiN barrier layer thicknesses in advanced HK/MG dielectric n-MOS FETs will be studied.

2. Experiment

For HK/MG transistors in this study, the dielectric consisted of 1.0 nm thermally grown SiO_2, the interfacial layer (IL), and 2.0 nm atomic layer deposited HfO_2 film. Next, various thicknesses of TiN (serving as a barrier layer) were deposited, followed by polycrystalline silicon (poly-Si) deposition. After removing the poly-Si gate, the samples were deposited on a 2.0 nm TaN layer and subject to PMA treatment at 450°C in oxygen ambient for 1 min. TiAl and TiN were subsequently filled as work function metal. The n-MOSFETs have drawn gate lengths of 0.03–1 um and drawn gate width of 0.3–10 um. Random telegraph noise (RTN) measurement in the HK/MG MOSFETs was performed with fast and accurate I-V characterization using an Agilent B1500 semiconductor parameter analyzer.

3. Results and Discussion

The measured I_D–V_D characteristics of the HK/MG device are given in Fig. 1 for the n-MOSFETs. In the Fig. 2, the interface trap density (N_{it}) was evaluated by the charge pumping measurement at 1 MHz. The I_D dependence on the TiN barrier thickness was observed. In addition, the I_D enhancement is related to the enhanced SiO_2/Si interface quality of the TiN barrier layer. As we can see from Fig. 2 in nMOSFET, 20Å TiN shows a lowest interface traps such that a highest drain current was obtained in Fig. 1. In other words, 20Å TiN sample has much better IL quality as a result of the lowest interface traps in its IL, as revealed in the charge pumping measurement results in the Fig. 2. The above dependency of the oxide quality on the TiN barrier layer thickness in n-channel MOSFET will be further examined as follows.

First, we need to determine the boundary between the high-k and the IL. The drain current random telegraph noise (I_D-RTN) measurement technique was used to determine whether the traps are located in the high-k layer or in the IL. A clear two-level I_D-RTN was observed and its histogram was analyzed. Fig. 3(a) and 3(b) show the measurement results for the n-MOSFETs. The discrete levels of I_D are attributed to the trapping/detrapping caused by an individual defect in the gate dielectric. The high current levels in the drain current correspond to the emission of electrons from the trap and the low current levels in the drain current correspond to the capture of electrons.

The value of $d\ln\langle\tau_c/\tau_e\rangle/dV_G$, i.e., the time constant variation rate, determines whether a trap is located in the HK dielectric or in the IL-layer, as shown in Fig. 4. The location of the trap in the dielectric is responsible for RTN and can be calculated as formula (1) [6]. Where τ_c and τ_e are the average capture time and emission time, respectively, q is the elementary charge, Tox is the physical thickness of the gate oxide, X_T is the distance of the trap from the Si-SiO_2 interface, q is the Boltzmann constant, and T is the absolute temperature. The time-constant variation rate depends on the gate voltage which shows a negative dependency. The result shows that the the defects in n-MOSFETs with various TiN barrier thicknesses are located in the HK. Therefore, carrier trapping/detrapping characteristics of the n-MOSFETs are controlled by the defects in the HK.

Next, we will examine the impact of the traps under the stress conditions of PBTI. During the oxidation annealing at high temperature, oxygen atoms can be diffused into TaN /TiN. Nitrogen atoms of TaN/TiN can be replaced by negative enthalpy of oxygen atoms and the replaced nitrogen atoms can be driven toward the interface of TiN/HfO_2. Then, the oxygen vacancy defects can be passivated to alleviate the electron trapping by the replaced nitrogen atoms from TaN/TiN [3]. The influence of oxygen diffusion on the TiN barrier thickness is significantly related to controlling the defects in HfO_2 dielectric under PBTI, as shown in Fig. 5-7. The results show that the threshold voltage (V_{TH}) shifts are strongly dependent on both stress electric field and TiN barrier thickness, as shown in Fig. 8. For thicker TiN barrier layer, more oxide defects can be passivated during oxidation annealing, then less electron trapping induces V_{TH} shifts during PBTI stress, as shown in Fig. 9.

4. Conclusion

This paper investigated and discussed the impact of PBTI on transistors with TiN barrier layers sandwiched between metal gate electrode and the HfO_2 dielectric. The use of TiN barrier layer is to improve the quality of HfO_2. This comes from the nitrogen passivation which replaced the oxygen diffused atoms through the TiN layer. The TiN barrier thickness influence on the oxygen diffusion is the root cause of the device degradation. A thicker TiN exhibits the best I_D improvement and lower N_{it} as a result of the passivation of the oxygen vacancy defects.

Acknowledgement

This work is partly supported by Taiwan National Science Council (NSC 100-2221-E-029-008-MY3).

References

[1] E. Cartier et al., IEDM (2011) 18.4.1.

[2] S. Krishnan et al., IRPS (2012) 5A.1.1.

[3] E. Cartier et al., Appl. Phys. Lett. 95 (2009) 042901.

[4] H. F. Chiu et al., Appl. Phys. Lett. 101 (2012) 122105.

[5] Y.-L. Yang et al., IEEE Electron Dev. Lett. 33 (2012) 1183.

[6] K. K. Huang et al., IEEE Electron Dev. Lett. 11 (1990) 90.

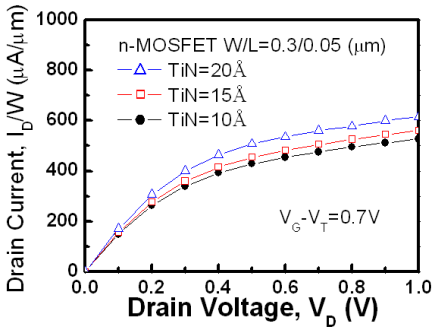

Fig. 1 I_D–V_D characteristics of HK/MG device for n-channel MOSFETs with various TiN barrier thicknesses.

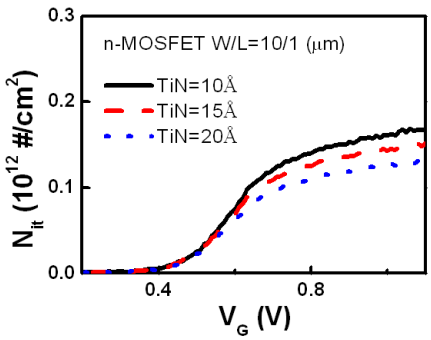

Fig. 2 The calculated Nit values of n-channel MOSFETs from the charge pumping measurements.

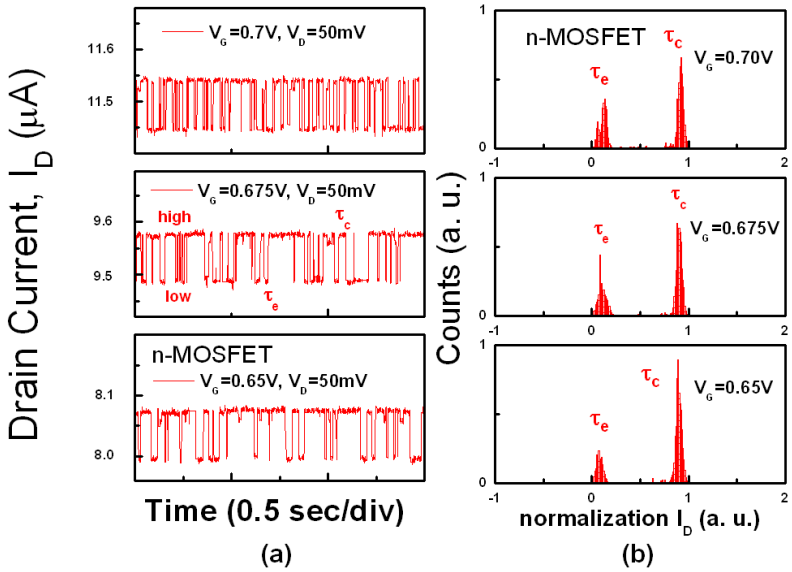

Fig. 3 (a) Two-level I_D-RTN in HK/MG n-channel MOSFETs and (b) its histograms.

Trap Depth:

$$\frac{d\ln\left\langle \frac{\tau_c}{\tau_e} \right\rangle}{dV_G} \times T_{ox} = -q \times \frac{X_T}{kT} \quad (1)$$

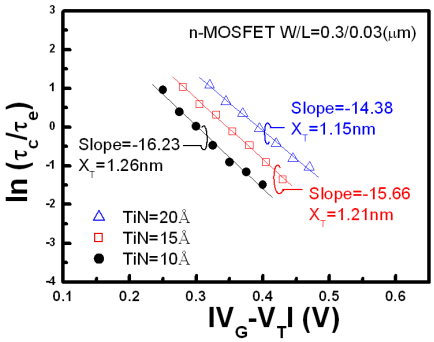

Fig. 4 Values of ln<τ_c/τ_e> vary with the gate overdrive voltage of the n-MOSFETs

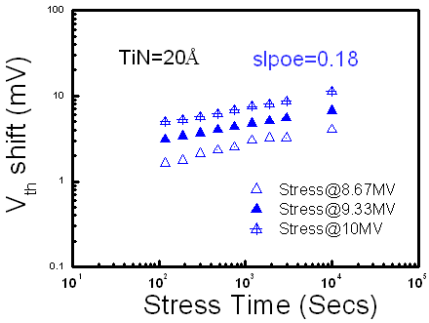

Fig. 5 The threshold voltage, V_{TH}, shift under different stress conditions for TiN= 20Å

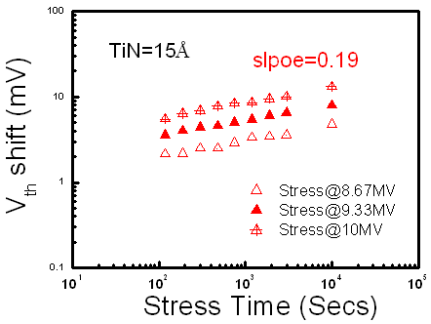

Fig. 6 The threshold voltage, V_{TH}, shift under different stress conditions for TiN= 15Å

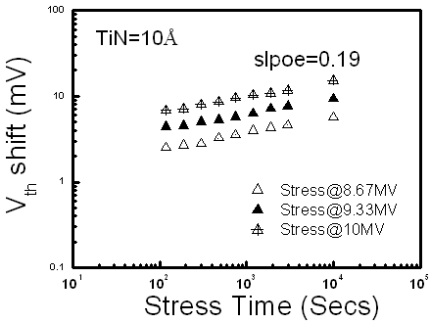

Fig. 7 The threshold voltage, V_{TH}, shift under different stress conditions for TiN= 10Å

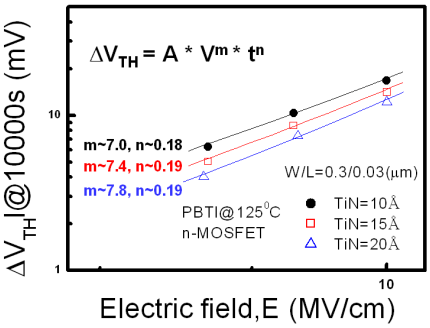

Fig. 8 The threshold voltage, V_{TH}, shift under different stress conditions with various TiN barrier thicknesses for PBTI in n-MOSFETs.

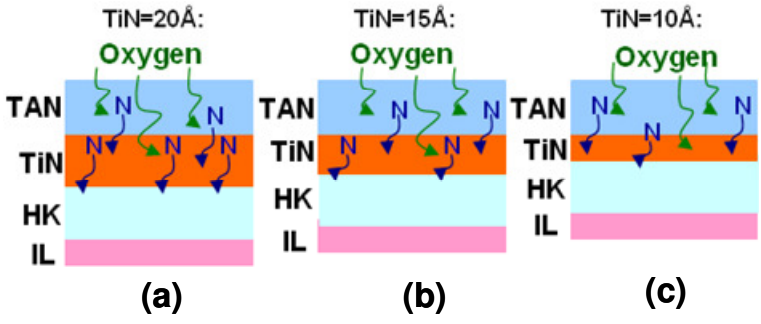

Fig. 9 The schematic illustrations show (a) TiN=20Å, (b) TiN=15Å and (c) TiN=10Å of the oxygen diffusing through TiN barrier by controlling the high-k vacancy defects during oxidation annealing.