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Measurement and analysis of annealing effect on parylene dielectric transistor

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Abstract

In order to understand the effect of annealing on parylene in organic thin-film-transistors (OTFT), we provide comprehensive experimental results on parylene dielectric OTFTs. We conducted electrical measurement, XRD and AFM for dinaphtho[2,3-*b* :2', 3'-*f*]thieno[3,2-*b*]thiophene (DNTT) based OTFT using parylene as gate dielectric. The results show annealing improves parylene crystallinity and enhances the OTFT mobility by 190 %.

1. Introduction

Organic devices have attracted wide interest for its flexibility, low temperature process and large area printability. There have been many reports on benefiting from this feature including flexible displays [1,2], flexible solar cells [3,4], and implantable electronic devices [5]. The key device in these applications is organic transistor, especially organic thin-film-transistor (OTFT), which allows us to access and drive flexible devices in large area by active matrix.

There have been several types of OTFT reported, using different structure and different materials. Bottom-gate bottom contact is a widely used structure because it can adapt to various process [2]. Bottom-gate top-contact on the other hand is known to have better mobility due better charge injection [6–8]. In this report we used bottom-gate top-contact structure.

Poly-p-xylylene (parylene) is a polymer dielectric material which is used as a gate dielectric. Parylene could be deposited with CVD process which is a low temperature process for the device. OTFT using parylene as gate dielectric has been reported to have good uniformity, good flexibility and relatively low operation voltage under -10 V [9,10]. Dix-SR, a type of parylene, was used in this report. Dix-SR was synthesized by KISCO.LTD and contains 94% of parylene-C but has higher thermal stability.

2. Experiment

We fabricated OTFTs on 75 um thick polyimide films. We first evaporated 50 nm of Au as gate by thermal vacuum evaporation. Then we CVD deposited parylene. The device was then taken in the oven and was annealed at 30, 80, 100 and 120℃ for 1h in air. Then we deposited 30 nm of dinaphtho[2,3-*b*:2',3'-*f*]thieno[3,2-*b*]thiophenes [11] (DNTT) a air-stable high mobility transistor material. DNTT was deposited by thermal evaporation. Finally we patterned 50 nm of Au as source and drain. Shadow mask were used for patterning Au and DNTT. Parylene was deposited without patterning.

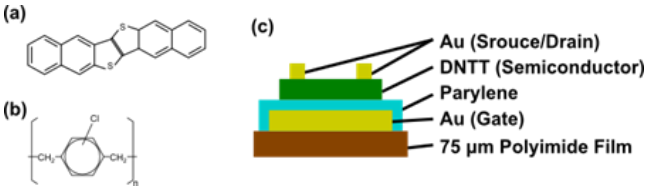

Fig.1 The chemical structures of (a) DNTT and (b) parylene. (c) Structure of bottom-gate top-contact OTFT

We performed basic electrical measurements on the device, including the transistor curve and flicker noise measurement. Agilent 4155C and E502B were use for these measurements.

Atomic force microscopy (AFM) measurement were performed on DNTT surface to see the morphological difference between DNTT layer deposited on top of parylene both with and without annealing. The measurement was done under room temperature in ambient air.

X-ray diffraction (XRD) profile was measured to see the annealing effect on parylene. The sample was prepared on glass substrates with 5 μm thick parylene layer on top. The sample was heated from 30℃ up to 150℃. The X-ray wave length used was 0.154 nm.

3. Result

Fig.2 (a) is the transistor characteristic of the transistor we fabricated. The mobility of the transistor was 0.30 cm^2/Vs. Fig.2 (b) shows the output characteristic of the device.

The mobility and the ON current of the device changed with annealing the parylene layer. The mobility of the device increased while the annealing temperature increased. The capacitance of parylene gate dielectric was 13.6 nF/cm^2 and was almost constant to annealing temperature. The maximum mobility was obtained by annealing the device at 100℃ and the measured mobility was 0.57 cm^2/Vs. The minimum flicker noise was seen when the device was

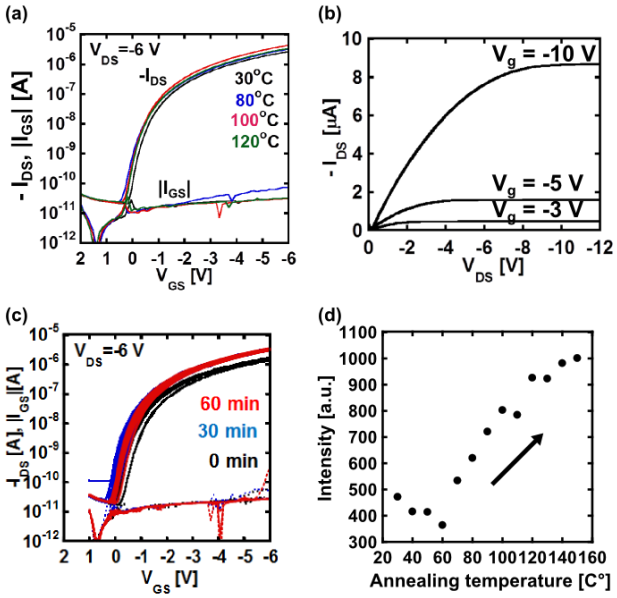

Fig.2(a) Transfer characteristics of device. (b) Output characteristics of device. (c) Device performance change with annealing time. (d) XRD peak intensity dependence at 2θ = 14.5˚with annealing temperature.

annealed at 100℃. The flicker noise was reduced by 56 % from the original value.

We also investigated the effect of annealing time of this device. We annealed the device at 100℃ for 30 and 60 min. The increase of ON current on 30 min annealed device compared to 60 min annealed device was little than the increase of device without annealing to 30 min annealed device (Fig.2 (c)).

XRD spectrum was taken on samples annealed at various temperatures. Every device had a peak at 2θ = 14.5˚ which is indexed as (020) crystallographic direction in parylene-C [12]. The peak intensity dependence with annealing temperature is shown in Fig.3 (d). The crystallinity of parylene starts increasing when it is annealed above 60℃ and kept increasing until it was annealed at 150℃.

AFM images of DNTT deposited on parylene are shown in Fig.3. The morphology and grain size of DNTT did not change with parylene annealing which means that the parylene annealing had no effect on DNTT structure.

4. Conclusion

Annealing increases the crystallinity of parylene. The XRD result indicated that crystallinity starts improving when parylene is annealed over 60℃. We have seen maximum improvement on mobility of OTFT by annealing the parylene gate dielectric at 100℃. The capacitance of parylene dielectric did not change by annealing which means the thickness of parylene is the same. The morphology of semiconductor layer also did not change by annealing which means the mobility enhancement was not caused by improvement on grain size of organic semiconductor.

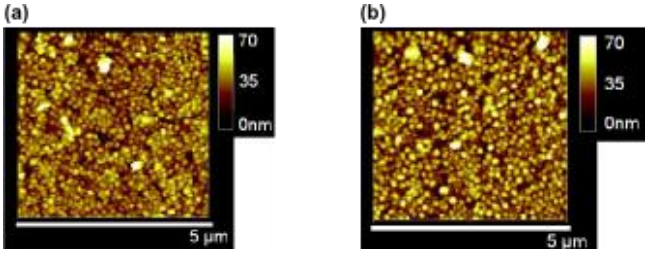

Fig.3 AFM image of DNTT surface (a) without parylene annealing and (b) with parylene annealing.

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