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Characterization of Electron Transport Properties of <110> InAs Nanowires by Hall Effect Measurements

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Abstract

We report on the characterization of electron transport properties of a single <110> InAs nanowire (NW). The carrier concentration and mobility of the NW have been quantitatively determinate with Hall effect measurement.

1. Introduction

With regards to the strong spin-orbit interaction (SOI), InAs is one of a promising candidate channel material of spintronics devices, particularly for Datta-Das spin field-effect transistors.[1] It is demonstrated that the relaxation of spins could be totally suppressed if the channel is oriented in one of the <110> axes.[2] Meanwhile, InAs NWs have outstanding promise for device applications because of their excellent electrical transport properties and according to the predictions of reduced spin relaxation in one dimension channel [3], InAs NW can provide a big advantage for the depression of spin relaxation. Therefore, we expected that InAs NW with <110> orientation is particularly attractive for spintronics, and investigations of their growth and transport properties are desirable.

In the previous study [4], we succeeded in the growth of <110> oriented InAs NWs, but their transport properties have not been studied so far. The evaluation of the free carrier concentration is crucial for the fabrication of spintronics devices on the nanometer scale, but their investigation in semiconductor NWs is carried out mainly with two-terminal devices, utilizing the field effect of the gate electrode. However, it has been confirmed that it overestimates the free carrier change considerably owing to many inherent uncertainties.[5][6] In this study, Hall bar devices were fabricated and Hall effect measurements and their temperature dependence were carried out on a single <110> NW.

2. Experimental procedures

We grew <110> InAs NWs by VLS process in a Riber MBE system using Pd catalyst on GaAs (111)B substrate. NWs grown along the <110> direction were confirmed by transmission electron microscopy [4], having stable zinc blende crystal structure without crystal imperfections such as wurtzite and stacking faults.

We fabricated Hall bar devices on a single <110> InAs NW with a following procedure. The grown NWs were detached from the substrate in DI water by a knife blade and dispersed onto heavily doped p-type Si substrate with a 300 nm thick SiO_2 layer and address markers. The precise positions of NWs were confirmed by scanning electron microscopy (SEM). Because the diameters of the NWs, which were around 150 nm, was relatively large and much thicker than metal film thickness of the electrodes, planarization process with HSQ layer was performed prior to electrodes formation. Thus, a HSQ layer, whose thickness is around 250 nm, was coated onto the NW dispersed substrates to cover the NWs. After hard baking, the NWs are uncovered again by reactive dry etching with CF_4 and O_2 that the height with only 50 ~ 100 nm from the top of the NW was exposed from HSQ layer. Prior to electrodes deposition of Ti(15 nm)/Pd(15 nm)/Au(10 nm), native oxide layer of NW was removed by dry etching with Ar gas. This yielded devices with contact resistance that was small compared to the channel resistance and independent of the temperature change. SEM image of the hall bar and its schematic are shown in Fig. 1. Four-terminal resistivity and Hall voltage measurement was carried out with a standard setup under different temperatures.

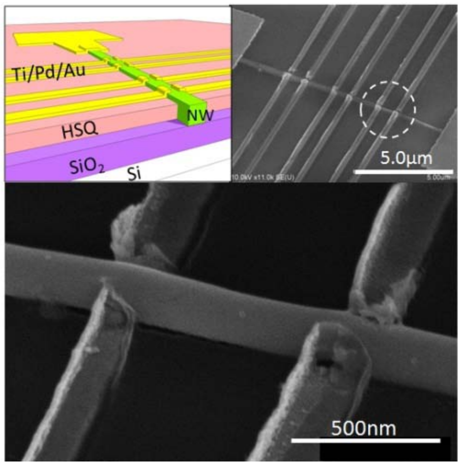

Fig. 1 Schematic and SEM images of Hall bar device.

3. Results and discussions

Figure 2 shows a Hall voltage V_H normalized to the drain current I_D as a function of magnetic field B measured at different temperatures. Each curve was shifted by 5Ω for clarity. The Hall voltage changes linearly with negative slopes as magnetic field B, which indicates that the NW is an n-type one. In 3D, the Hall voltage V_H can be expressed as

$$V_H = -\frac{I_D w_H}{qnS} B \qquad (1)$$

where w_H is the distance between Hall voltage terminals, q is the elementary charge, n is the electron concentration and S is the cross sectional area. We used the same expression for NWs and calculated the electron concentration and Hall mobility by combining four-terminal resistivity measurement.

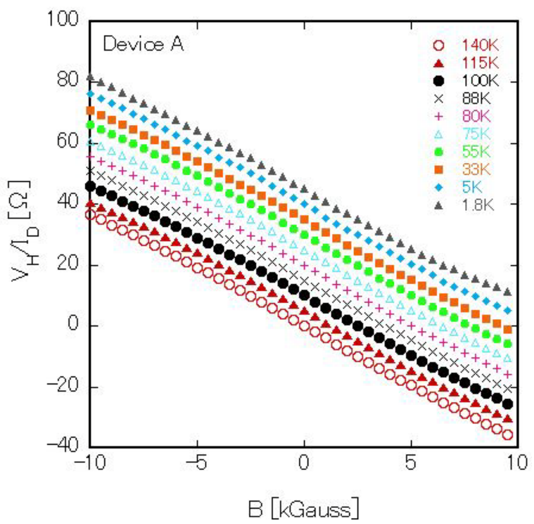

Fig. 2 Ratio between Hall voltage and drain current of sample A as a function of magnetic field.

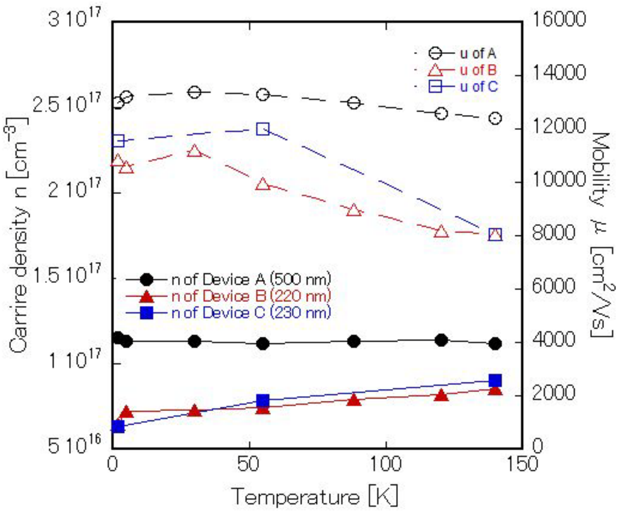

Fig. 3 Temperature dependent carrier density and mobility.

Figure 3 shows the temperature dependent carrier density and transport properties of three devices with different diameter of NW. The carrier concentrations are almost independent of temperature below 140 K for all three devices, and the mobility shows a gradual enhancement of the mobility from 140 K to 30 K and saturation below 30 K.

The weak temperature dependence of carrier density could be explained by the electron accumulation occurred at the surface of NW, which is due to the pinning of the Fermi level above the conduction band [7][8] and to the formation of 2D electron gas. At low temperature, these electrons at surface dominated the carrier concentration rather than the electrons in the bulk region.

Increase of Hall mobility from 140 K to 30 K is mainly attributable to the reduction of phonon scattering, and below 30K, the ionized impurities scattering or surface roughness scattering dominated over other scattering events. Since our NWs were not intentionally doped, impurity scattering should not be a factor. As we have discussed above, the electron transport near the surface dominated the electrical characteristics. Therefore, we attributed that the temperature dependency of carrier mobility mainly caused by surface roughness scattering which would produce weak temperature dependence [9]. It is also likely that fluctuation of the surface impurity or surface states also give rise to fluctuation of the surface potential and to the electron scattering similar to the surface roughness scattering. [10]

Our study also aims at demonstrating superiorities of electrical transport within these NWs, thus back gate transistor structure was fabricated. Field effect mobility of 6150 cm^2/Vs was estimated by back gate measurement at room temperature which is higher than our <111>-oriented NW sample.[11]

4. Conclusions

In summary, we proposed <110> InAs NWs as channel material of spintronics devices and grown these NWs by VLS process using Pd catalyst. Specifically, carrier density and mobility of single NW were investigated by utilizing Hall measurements at different temperatures, and superiorities of electrical transport properties were suggested as compared to <111>-oriented NWs as well.

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