Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials, Tsukuba, 2014, pp362-363

Hot carrier effect and PBTI of a thin-film SOI power MOSFET at high temperature

Wataru Yoshida, Tomoya Takasugi, and Satoshi Matsumoto

Kyushu Institute of Technology,
Sensui-cho, Tobata-ku, Kitakyushu-shi, Fukuoka, 804-8550, JAPAN
Phone/Fax:+81-93-884-3268, e-mail:o349535w@mail.kyutech.jp

Abstract

This paper describes the hot carrier effect and positive bias temperature instability (PBTI), of a thin-film SOI power MOSFET at high temperature. The device degradation, which is caused by hot carrier effect and PBTI, depends on temperature. Device degradation is different for stress gate bias condition. Device degradation caused by hot carrier effect occurs at lower stress gate voltage and caused by PBTI occurs at higher stress gate voltage. Degradation of the on-resistance reduces as temperature increases at lower gate stress voltage. Threshold voltage shift shows the maximum when temperature is 473 K at lower stress gate voltage. Degradation of on-resistance enhances and threshold voltage shift increase with increasing temperature at higher stress gate voltage.

1. Introduction

Recently, high-temperature applications of power MOSFETs and ICs have attracted attention owing to the increase in their demand for applications in various fields such as automobiles, aerospace industries, and nuclear power plants [1]. The thin-film SOI power MOSFET is one of the promising candidates because it can avoid thermally induced latch-up and realize lower leakage current[2].

We previously reported device characteristics and design guidelines of the thin-film SOI power MOSFET at high temperature [3][4]. For practical use, hot carrier effect and positive bias temperature instability (PBTI) will become key issues for high temperature applications. However, those for the thin-film SOI power MOSFETs at high temperature are not clear.

This paper clarifies temperature dependence of hot carrier effect and PBTI of the thin-film SOI power MOSFETs at high temperature.

2. Device structure and Fabrication process

The schematic cross section of the fabricated thin-film SOI power MOSFET is shown in Fig. 1. The body contacts were formed to suppress the parasitic bipolar effect and the main structural parameters are listed in Table 1. The SOI power MOSFET was fabricated using 0.5 μm-rule polycide gate process with LOCOS isolation.

Main device characteristics are listed in Table 2. On-resistance at 300K is larger than that at 573K and, on the contrary, the threshold voltage at 573K is larger than that at 300K.

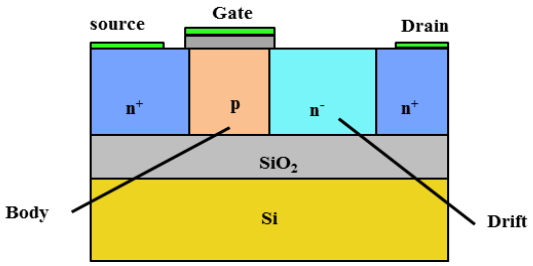

Fig. 1 Schematic cross section of SOI power MOSFET

Table I The main structural parameters

Top Si layer [μm]	0.14
Buried oxide [μm]	0.4
Gate oxide [nm]	11
Channel Length [μm]	0.8
Drift Length [μm]	0.5
Channel Width [μm]	100

Table II Device characteristics

	Temperature [K]	
	300	573
On-Resistance [Ω]	179	408
Threshold Voltage [mV]	610	360
Breakdown Voltage [V]	14.1	6.38

3. Result & Discussion

Dependence of degradation rate of on-resistance on stress gate voltage is shown in Fig. 2. Stress time is 3,600 sec.

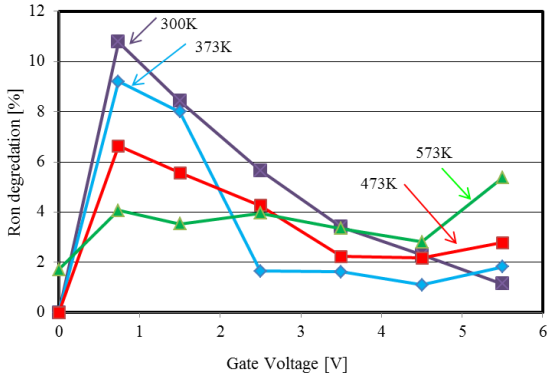

Fig. 2 Dependence of degradation rate of on-resistance on stress gate voltage

and stress drain voltage is 6 V. Degradation of the on-resistance occurs even at the gate voltage of 0 V when temperature is 573 K. This is caused by increased leakage current at high temperature. There are two kinds of degradation of on-resistance. The one is degradation near threshold voltage. In this case, degradation rate of on-resistance decreases with increasing temperature. The degradation of on-resistance is caused by the hot carrier injection into gate edge of the drift region [6]. Injection of the hot carrier reduces as temperature increases because the impact ionization coefficient decreases as temperature increases. Furthermore, trapped hot carriers are released in high temperature caused by high temperature annealing effect and this annealing effect accelerates as temperature increases. Thus, degradation of on-resistance is suppresseed.

The other is degradation at high stress gate voltage (>5.5 V). The degradation rate of on-resistance increases with increasing temperature. In this case, the high electric field appears in channel region. This promotes positive bias temperature instability (PBTI). PBTI is enhanced by high electric field and high temperature. In addition, the electric field at 573 K is higher than that at 300K. Thus PBTI at 573 K accelerate.

At 573 K, degradation rate of on-resistance is almost constant regardless of gate voltage when gate stress voltage is less than 4.5 V. This is caused by drain avalanche hot carrier injection, PBTI and high temperature annealing effect. The drain avalanche hot carrier effect reduces and annealing effect enhances with increasing temperature. Thus the degradation of the on-resistance suppresses as temperature increases. On the other hand, degradation of on-resistance caused by PBTI increases with increasing gate voltage and temperature. The threshold voltage shift at 573 K is the highest when the stress gate voltage is 5.5 V. This is caused by PBTI and PBTI increases with increasing temperature.

Dependence of threshold voltage shift on stress gate voltage is shown in Fig. 3. The stress drain voltage is 6.0 V.

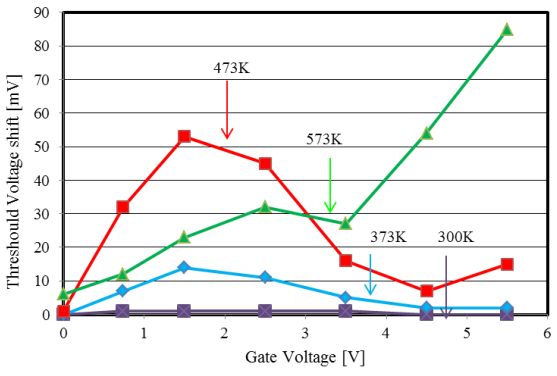

Fig. 3 Dependence of the stress gate voltage on threshold voltage shift

The threshold voltage shift is not observed at room temperature. This shift occurs even at the gate voltage of 0 V when temperature is 573 K. This is caused by increased leakage current at high temperature. We can see two kinds of threshold voltage shift. When gate stress voltage is near 1.5 V, the threshold voltage shift increases with increasing temperature and excessive increase in temperature reduces threshold voltage shift. In this case, drain avalanche hot carrier injection induces threshold voltage shift. On the other hand, threshold voltage shift caused by hot carrier effect is recovered by high temperature annealing effect and this effect enhances with increasing temperature. Therefore threshold voltage shift at 573K is lower than that at 473K.

When the gate stress voltage is high, threshold voltage shift increases with increasing temperature. In this case, PBTI promotes threshold voltage shift.

4. Conclusions

The temperature dependence of hot carrier effect and PBTI of a thin-film SOI power MOSFET has experimentally investigated. The threshold voltage shift and degradation of the on-resistance occur even at the gate voltage of 0 V when temperature is 573 K. Degradation of on-resistance decreases with increasing temperature at lower stress gate voltage. These degradation are combination of drain avalanche hot carrier injection, channel hot carrier injection, PBTI, and high temperature annealing effect. Degradation of on-resistance increases with increasing temperature at high stress gate voltage. This degradation is caused by PBTI. The threshold voltage shift increases with increasing temperature at high gate stress voltage. This is caused by PBTI. The threshold voltage shift has the maximum value when the gate stress voltage is near 1.5 V. This is caused by combination of drain avalanche hot carrier injection, channel hot carrier injection, high-temperature annealing effect and PBTI.

References

[1] C. Buttay, D. Planson, B. Allard, D. Bergogne, P. Bevilacqua, C. Joubert, M. Lazar, C. Martin, H. Morel, D. Tournier, and C. Raynaud, Mater. Sci. Eng. B, **176**, 283 (2011) .

[2] J. P. Colinge: *Silicon-on-Insulator Technology: Materials to VLSI* (Kluwer, Dordrecht, 2004) 3rd ed., p. 200.

[3] Y. Morisawa, T. Kodama, and S. Matsumoto: Microelectron. Reliab. **52**, 2380 (2012).

[4] M. Yoshimura, A. Uchida and S. Matsumoto: Microelectron. Reliab., **53**, 1778, 2013.

[5] E. Amat, T. Kauerauf, R. Degrave, R. Rodriguez, M. Nafria, X. Aymerich, and G. Groeseneken, IEEE Trans. Electron Device, **56**, 454, (2009).

[6] S. Matsumoto Jpn. J of Appl. Phys 47, 8739, (2008).