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Effect of Gate Oxide Process at SiC-MOS Interface on Threshold Voltage Shift Analyzed by DLTS

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Abstract

The influence of nitridation and wet oxidation following nitridation on near-interface-traps in SiC-MOSFETs was analyzed by deep level transient spectroscopy (DLTS). We established a method to evaluate the space distribution of traps. From the DLTS measurements, we found that traps at the shallow levels affect subthreshold swing and mobility of SiC-MOSFETs after the wet oxidation, while threshold voltage shift was influenced by deep level traps which increased after the wet oxidation. By measuring the spatial distribution of the deep level traps, it was revealed that they were increased in the SiC bulk near the interface by the 800 °C and 900 °C wet oxidation, while the traps at the MOS interface increased only after the 900 °C wet oxidation. It is expected that these variations in the trap densities correspond to the degree of the threshold voltage shifts observed in SiC-MOSFETs.

1. Introduction

SiC-MOSFETs are required to be designed to have a large threshold voltage (V_{th}) for prevent erroneous arc firing in circuits. Although V_{th} is usually controlled by doping concentration in the channel, it makes the mobility to be lower. Recently, Furuhashi et al [1] have reported that it is possible to obtain the V_{th} positive shift by a wet oxidation process after nitridation of a gate oxide without significant decrease of the mobility. The reason, however, of the phenomena has not been clarified. In this study, to shed light on the mechanism, we investigated the influences of the nitridation and the wet oxidation following the nitridation on near-interface-traps in SiC-MOSFETs by deep level transient spectroscopy (DLTS). We established a DLTS method to evaluate the space distribution of traps including interface, with controlling a pulse voltage height to fix the surface potential variation $\Delta\psi_s$, while sweeping a bias voltage. The spatial distribution of the deep level traps affected by the nitridation and wet oxidation at different temperatures were analyzed , and it was found the relation between the threshold voltage shift and trap densities in SiC bulk at the interface.

2. Experimental

Frist, a gate oxide layer was formed by high temperature dry oxidation on Si-face 4H-SiC. Then, nitridation was done by NO annealling, after which 800°C or 900 °C wet oxidation was performed for 30 min. Then, MOS-FET structures were fabricated by electrode formation. n-type MOS-capacitors processed under the same nitridation/oxidation conditions as the MOS-FETs were fabricated and the near-interface-trap densities and space distribution of traps were analyzed by DLTS measurements.

3. Results and Discussion

Figure 1 shows I_dV_g characteristics and field-effect mobilities μ_{fe} (300 K, V_d = 0.1 V). Subthreshold swing (SS) and μ_{fe} were 1600 mV/dec and 3 cm^2/V/s, respectively, after the dry oxidation, and these values were improved to 500 mV/dec and 26 cm^2/V/s, respectively, after the nitridation. The 800 °C wet oxidation after the nitridation shifted V_{th} by +0.75 V, while SS and μ_{fe} were not significantly changed, only 1.1 and 0.92 times, respectively. The wet oxidation at a higher temperature of 900 °C resulted in a larger V_{th} shift (+4.0 V) and degradation of both SS and μ_{fe}.

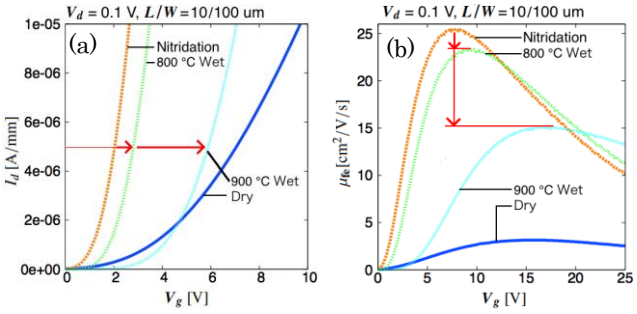

Fig. 1 The characteristics of MOSFET (a) I_dV_g characteristics and (b) Field effect mobility μ_{fe}

For comparison, we examined the near interface trap density (D_{it}) of the MOS capacitors by a Hi-Lo CV method at 300 K as shown in Fig. 2(a). The densities of traps having variety of time constants (τ = 1 μs ~ 1 s) were measured from the difference between the quasi-static CV (QSCV) and 1 MHz CV characteristics. The time constant values correspond to energy levels of E_c - E_t = 0.35 ~ 0.7 eV (for

300 K and cross capture section $\sigma = 10^{-14}$ cm^2). By the 800 °C wet oxidation following the nitridation, the density of traps deeper than 0.35 eV were increased. The increasing of the deep level traps is thought to contribute to the V_{th} positive shift without the mobility degradation [2].

To measure the shallower level traps than 0.3 eV and define the time constant and space distribution of the traps, we measured D_{it} by DLTS. Figure 2(b) shows the D_{it} of the MOS capacitors obtained from the DLTS signals. A reverse bias was applied for depletion layer width to be 300 nm, and a pulse bias (flat band voltage + 2 V) was applied to accumulate electrons. The rate window was $\tau = 0.88$ ms and the measurement temperature was 80 ~ 400 K. We can measure the density of 0.10 ~ 0.75 eV energy level traps (for the case of $\sigma = 10^{-14}$ cm^2) under these measurement conditions. D_{it} was decreased 0.25 times at all around the energy level by the nitridation. The variation of D_{it} after the 800 °C wet oxidation has difference between the shallower and deeper traps than 0.2 eV. After the 900 °C wet oxidation, the D_{it} including shallow traps increased by a factor of 2 comparing to the nitridation sample. The amount of D_{it} at the shallow levels (< 0.2 eV) is likely to correspond to the variations of SS and mobility shown in Fig. 1, while D_{it} at the deeper levels (> 0.2 eV) affect the V_{th} shift, in agreement with the result by the Hi-Lo CV method in Fig. 2(a).

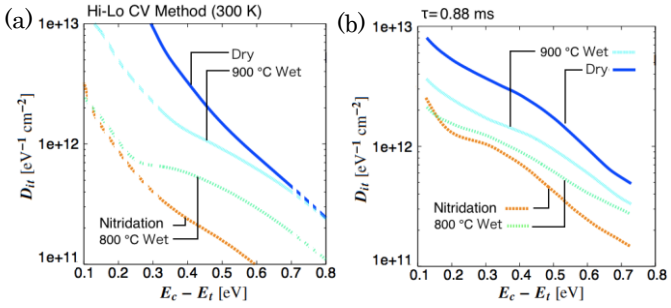

Fig. 2 Density of the near interface traps in the MOS capacitor measured by (a) Hi-Lo CV method (b) DLTS

We measured the space distribution of the deep level traps from the interface to SiC bulk by the bias dependence of the DLTS signal to further reveal the correlation between D_{it} at the deep levels and V_{th} shift. The relationship between surface potential ψ_s and bias voltage V_g was calculated from QSCV and 1 MHz CV characteristics [3]. Then, the pulse voltage height was controlled to fix the surface potential variation $\Delta\psi_s = 0.1$ eV, while sweeping the bias voltage. The large pulse height was applied to bend the band structure of the flat-band or accumulation mode MOS structure. By using this method, we can obtain the DLTS signals irrespective of the state of MOS structure, i.e. depleted, flat-band, and accumulated. Thus, the space distribution of the traps at SiC bulk and interface can be estimated.

Figure 3 shows the bias voltage dependence of the DLTS signal at 300 K. The horizontal axis indicates the surface potential when the pulse voltage was applied $\psi_s = \psi_p$. (The bias voltage was applied to make $\psi_s = \psi_p$ - 0.1 eV). And the vertical axis indicates the DLTS signal $\Delta C = C(e\tau)$ - $C(\tau)$, normalized by C_{ox}. The rate window (τ) was set to the same value of 0.88 ms as the measurement in Fig. 2(b), and this τ value corresponds to an energy level of 0.5 eV (for $\sigma = 10^{-14}$ cm^2). The signals of $\psi_p < 0$ eV show traps in the SiC bulk near the edge of the depletion layer and the signal of $\psi_p \sim 0$ eV indicates the interface traps.

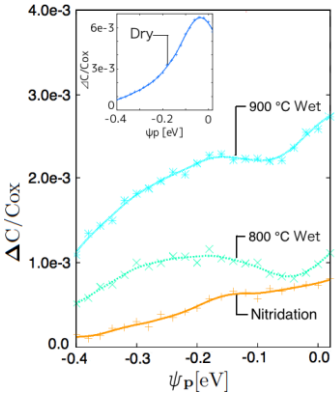

Fig. 3 Bias dependence of DLTS signal ($\tau = 0.88$ ms), ψ_p is the surface potential when the pulse voltage is applied.

There is a peak around $\psi_p \sim -0.05$ eV after the dry oxidation and the peak disappeared by the nitridation. The DLTS signals at $\psi_p < 0$ eV (SiC bulk near the interface) increased after the 800 and 900 °C wet oxidations. The traps at the interface do not change largely at 800 °C wet oxidation, while they increased after the 900 °C wet oxidation. And after the 900 °C wet oxidation, the $\psi_p \sim 0$ eV signals (interface) became three times higher than that after the nitridation. The observed DLTS signal variations imply that the deep level traps of the SiC bulk was increased in wide depth range depending on the temperature of the wet oxidation, and that the deep level interface traps were increased after the 900 °C wet oxidation. Therefore, it is speculated that the traps in the SiC bulk caused the small V_{th} shift after the 800 °C wet oxidation, and that the increase of the traps both in the SiC bulk and interface led to the large V_{th} shift after the 900 °C wet oxidation.

4. Conclusions

In this study, the influences of the nitridation and the wet oxidation following nitridation on near the interface trap were analyzed by DLTS. The shallower traps than 0.2 eV and deep level interface traps were decreased by nitridation. By 800 °C wet oxidation following nitridation, the shallower traps was not increased. After 900 °C wet oxidation following nitridation, the deep level interface traps were increased. Moreover, the deep level traps in the SiC bulk were increased by 800, 900 °C wet oxidation. These variation correspond with the Subthreshold swing and the mobility variation and the threshold voltage shift.

References

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