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Quantitative Characterization of Border Traps with Widely-Spread Time Constants in SiC MOS Capacitors by Transient Capacitance Measurements

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Abstract

The method to determine the border trap density in MOS capacitors was proposed and demonstrated, by taking account of the wide distribution of time constants. Border trap state densities around 10^{11} - 10^{12} $cm^{-2}eV^{-1}$ were estimated for some of the test samples of 4H-SiC MOS capacitors.

1. Introduction

The capacitance-voltage (*C-V*) characteristics of SiC MOS capacitors with thermal oxides are often suffered from a significant stretch-out and frequency dispersion in the accumulation region. One of the possible models for this phenomenon is the effects of "border traps" in oxide [1], however, the quantitative analysis of these traps has not been established, though there have been a few reports on the method by impedance analysis on InGaAs MOS interface [2]. In this study we propose a method to estimate the density of border traps in SiO_2/SiC MOS capacitors by transient capacitance measurement. We assume the oxide trap model [3], in which carriers in semiconductors interact with the traps in oxide by tunneling. One of the remarkable characteristics of this model is the widely-spread response time of the traps, due to the variation of the tunneling distance between the interface and the traps, as schematically shown in **Fig. 1**.

2. Analysis of Transient Response of Capacitance

Transient response of capacitance (*C-t*) gives the information of trapping behaviors of the carriers in MOS capacitors [4, 5], since the change of amount of trapped charges shifts the *C-V* curve. Taking account of the widely-spread time constants of the traps due to their depth distribution in oxide, the time-dependent change of capacitance (ΔC) would be described by "extended-Debye relaxation model" [6], instead of a conventional relaxation with a single time constant. When a voltage bias on capacitor suddenly shifts at $t = 0$, ΔC is expected to be described by,

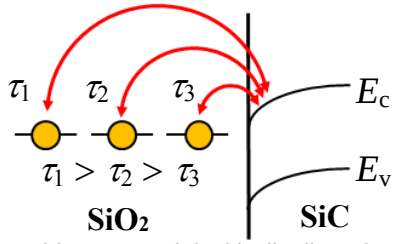

Fig. 1 The oxide trap model with distributed response time, which is dependent on distance between traps and the interface.

$$\Delta C \equiv \left|C(t) - C_{\mathrm{eq}}\right| \cong \left|\Delta C_0\right| \exp\left[-\left(\frac{t}{\tau_{\mathrm{eff}}}\right)^{\beta}\right] \qquad (1)$$

where C_{eq} is the capacitance in thermal equilibrium, β is the stretched exponential factor ($0 < \beta < 1$) of the response time, τ_{eff} is the effective relaxation time of the group of traps with distributed response time, and ΔC_0 is the total change of capacitance caused by the trapped charges. In this study, the gate bias on capacitors is kept in accumulation state ($V_g = V_{trap}$) for a period of time (T_{trap}) to fill the traps, before a sudden shift to the near-flatband state ($V_g = V_{meas}$) to observe *C-t* characteristics. This method is similar with the one demonstrated in ref. [5] for Ge MOS. The obtained *C-t* characteristics are fitted by Eq. (1) to determine ΔC_0, from which the amount of trapped charges in border traps per area (Q_{bt}) is estimated, assuming that the distance of the traps from the interface is significantly shorter than the film thickness.

3. Fabrication of 4H-SiC MOS Capacitors

Three kinds of MOS capacitors, A, B, and C, were fabricated on 4H-SiC wafers with ~1×10^{16} cm^{-3} doped n-type epitaxial layers, by thermal oxidation at 1300°C in dry O_2. Samples A and B were fabricated on (0001) face by 1-atm-O_2 oxidation, while sample C is on (000-1) face, prepared by 0.02-atm-O_2 oxidation. The oxide thicknesses for these samples were ~14 nm in common.

4. Results and Discussions

As shown in **Fig. 2**, the sample A showed nearly-ideal *C-V* characteristics [7] while the sample B resulted in a stretched-out curve even though these two were prepared in nominally the same condition (the reason for this difference is unidentified). The sample C showed a

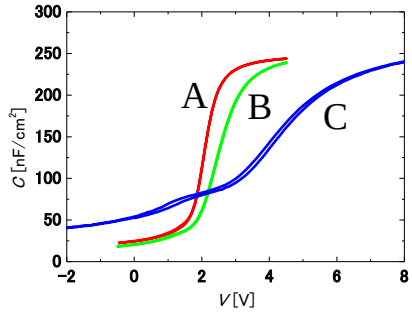

Fig. 2 1 MHz bidirectional *C-V* characteristics of three SiC MOS capacitors: A, B, and C. The samples A and B were fabricated on (0001) face and oxidized by 1-atm-O_2. The sample C was fabricated on (000-1) face and oxidized by 0.02-atm-O_2.

more stretched-out curve which indicates the existence of more border traps in the oxide. The typically observed *C-t* characteristics are shown in **Fig. 3 (a)**. Data for the samples B and C are well-fitted by Eq. (1), by selecting appropriate parameters: β, τ_{eff}, and ΔC_0. In contrast, the sample A showed a transient behavior to the opposite direction. We speculate that the significantly low density of border traps in this sample revealed the effects of hole trapping in oxide.

We confirmed that the deduced parameters (β, τ_{eff}, and ΔC_0) do not change significantly even when we changed T_{trap} from 1 to 1000 s. In the following experiment we employed T_{trap} = 100 s, which is sufficiently long for the electrons to fill the traps during the electrical stress. The *C-t* characteristics obtained for different V_{trap} are shown for samples B and C, in **Fig. 3 (b)** and **(c)**, respectively. From the estimated Q_{bt} for each V_{trap}, the density of states of

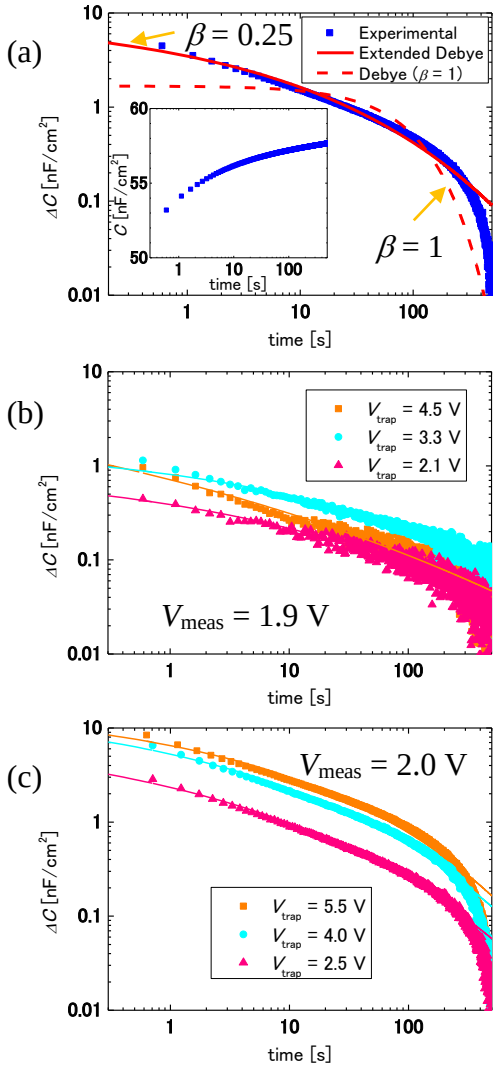

Fig. 3 (a) The typical *ΔC-t* characteristics with fitted curve by Eq. (1) (sample C, V_{trap} = 4.5 V, V_{meas} = 1.9 V). The curve corresponding to a conventional Debye system is also shown by broken line for a comparison. The inset shows the raw data of transient response of capacitance. **(b)** *ΔC-t* characteristics of sample B for various V_{trap}, with fitted curves by Eq. (1), and **(c)** those of sample C.

border traps (D_{bt}) was determined by,

$$D_{bt} \cong \frac{1}{q}\frac{dQ_{bt}}{d\varphi_s} \qquad (2)$$

where φ_s is the surface potential of SiC, and q is the elementary charge. The estimated D_{bt} values are plotted in **Fig. 4** for samples B and C, which are in the order of 10^{11} - 10^{12} $cm^{-2}eV^{-1}$ for a wide range of energy. Sample C shows approximately one order of magnitude greater D_{bt} than sample B, which is consistent with larger stretch-out of *C-V* characteristics of Sample C. To our knowledge this is the first demonstration of a quantitative evaluation of the border traps density in SiC MOS capacitors. Most of the data suggested that τ_{eff} values are in the order of 10^0 - 10^1 s for a wide range of energy, which is suggesting that the active border traps mainly distributes within ~1 nm from the interface if we assume the tunneling mass of electrons in SiO_2 [8].

5. Conclusions

The method to determine the border trap density in MOS capacitors from transient capacitance characteristics was proposed and demonstrated, by taking account of the wide distribution of time constants. D_{bt} around 10^{11} - 10^{12} $cm^{-2}eV^{-1}$ was estimated for the 4H-SiC MOS capacitors with poor *C-V* characteristics while quite a different transient characteristics observed for the capacitor with nearly-ideal *C-V* characteristics.

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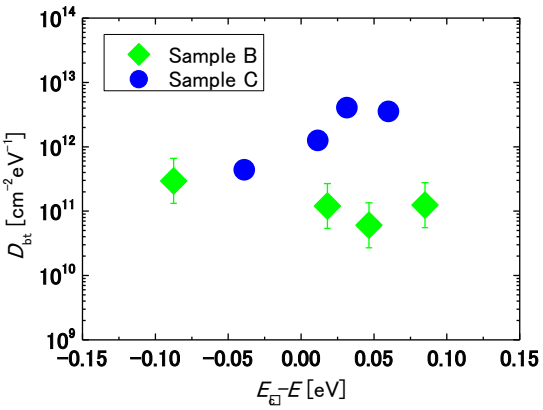

Fig. 4 Estimated densities of states of border traps in samples B and C.