Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials, Tsukuba, 2014, pp364-365

Well Proximity Effect Impact on Fully Isolated Low R_{on}*Q_g MOSFET Performance

Masashi Shima, Masaya Katayama, Hidekazu Sato, Michihiro Onoda, Tetsuo Yoshimura, Toshihiro Ishihara, Yoshiyuki Suzuki and Noriyuki Suzuki,*Masayuki Hosoda, *Tadahiro Imada, *Tatsuya Hirose

Fujitsu Semiconductor Limited
1500 Mizono, Tado, Kuwana Mie 511-0192, Japan
Tel: +81-594-24-9168 E-mail: masashima@jp.fujitsu.com
*Fujitsu Laboratories Ltd.
10-1 Wakamiya, Morinosato, Atsugi Kanagawa 243-0197, Japan

Abstract

We have developed a fully isolated low R_{on}*Q_g lateral N/PMOS with shallower and deeper profile wells used for a core or a high voltage gate logic transistor. A surface concentration due to well proximity effect was for the first time found to have a large impact on the characteristic and deviation of a low R_{on}*Q_g lateral transistor with a 20V breakdown voltage. A well being formed far from a drift region and close to a source region suppressed a surface concentration due to well proximity effect in a drift region to improve R_{on} and reduced the junction electric field to increase a breakdown voltage. Characteristic deviation in the low R_{on} NMOS was also reduced, while not in the PMOS. A fully isolated NMOS with a well layout optimized to improve R_{sp}-BV_{dss} has successfully achieved a competitive R_{sp} of 6.8mΩ-mm^2 and R_{on}*Q_g of 37mΩ-nC compared to previously reported lateral NMOSs. These results indicate that well layout and proximity effect must be cared to optimize figure of merits of low voltage transistors integrated in PMICs for portable electric products.

Introduction

The requirements for PMICs in portable applications are a high efficiency, a high current capability, and a compatibility with a standard fabrication process of logic transistors [1]. For a low-cost solution, we have proposed and developed fully isolated 20V breakdown voltage low R_{on}*Q_g N/PMOS transistors with shallower and deeper profile wells used for a core or a high voltage gate logic transistor. The fully isolated NMOS transistor can minimize substrate injection when negative transients below substrate bias because the two connected pwells can electrically isolate the drain from the deep-nwell. A well edge position is a critical parameter in this kind of transistor because a surface concentration due to well proximity effect (WPE) has a large impact on performance, such as specific on-resistance (R_{sp}) and breakdown voltage (BV_{dss}) [2]. In this paper, impact of WPE on fully-isolated 20V breakdown voltage low R_{on}*Q_g transistor is analyzed for the first time and an optimum well layout is discussed from a practical point of device performance and its deviation in a wafer.

Device characteristics

Fig1 shows a simulated dependence of avalanche breakdown distribution in NMOS at gate bias of 0V. Surface concentration due to WPE distributes around an edge of shallower profile pwell (pwell1). When pwell1 edge exists in a drift region, a surface concentration due to WPE decreases the depth of a drift region to increase R_{on} and increases electric field at a LDD/pwell1 junction to occur avalanche breakdown there. As pwell1 edge moves from a drift region to a channel region, the depth of a drift region increases and maximum avalanche position changes from the junction to the shallower position just under the gate edge. Fig. 2 shows dependence of V_t, R_{on}, BV_{dss} on the pwell1 edge position in NMOS and PMOS. The pwell1 existing in channel region increases V_t and BV_{dss} while decreases R_{on} below data without WPE. A reduction of R_{on} in spite of an increase in V_t and thus channel resistance is considered to be attributed to a reduced surface concentration due to WPE in a drift region and thus reduced parasitic resistance. A PMOS, which suffered the maximum surface concentration due to WPE at nwell edge position, showed almost the same dependence as an NMOS. Fig.3 shows the dependence of characteristic deviation on the shallower well edge position. In NMOS, V_t deviation increased when pwell1 edge existed close to the source region, while R_{on} deviation decreased after increase until pwell1 edge moved close to the gate edge from the drift region. On the other hand, decrease in R_{on} deviation was not observed in PMOS when the nwell edge existed close to the source region. Larger component of channel resistance sensitive to Vt deviation in PMOS is considered to be the reason. Fig.4 shows a benchmark of figure of merits of reported lateral NMOSs. Competitive R_{sp} of 6.8mΩ-mm^2 and R_{on}*Q_g of 37mΩ-nC have been achieved compared to previous lateral device technologies owing to an optimum well layout.

Conclusions

A surface concentration due to WPE was found to have a large impact on the performance of a low R_{on}*Q_g lateral transistor with a low breakdown voltage of 20V. These results indicate that well layout and proximity effect must be cared to optimize figure of merits of low voltage transistors integrated in PMICs for portable electric products.

References

[1] Z.J. Shen, et al.,"Lateral Discrete Power MOSFET:Enabling Technology for Next-Generation, MHz-Frequency, High-Density DC/DC Converters", Proc. APEC, pp. 225–229, 2004

[2] P. G. Drennan, et al.,"Implications of Proximity Effect for Analog Design", IEEE Custom Integrated Circuits Conf., pp. 169–176, 2006

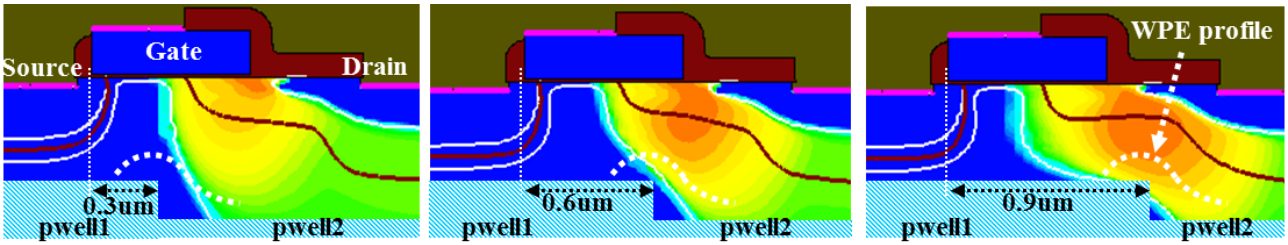

Fig. 1: Simulated dependence of avalanche breakdown on the pwell1 edge position in NMOS at Vg=0V.

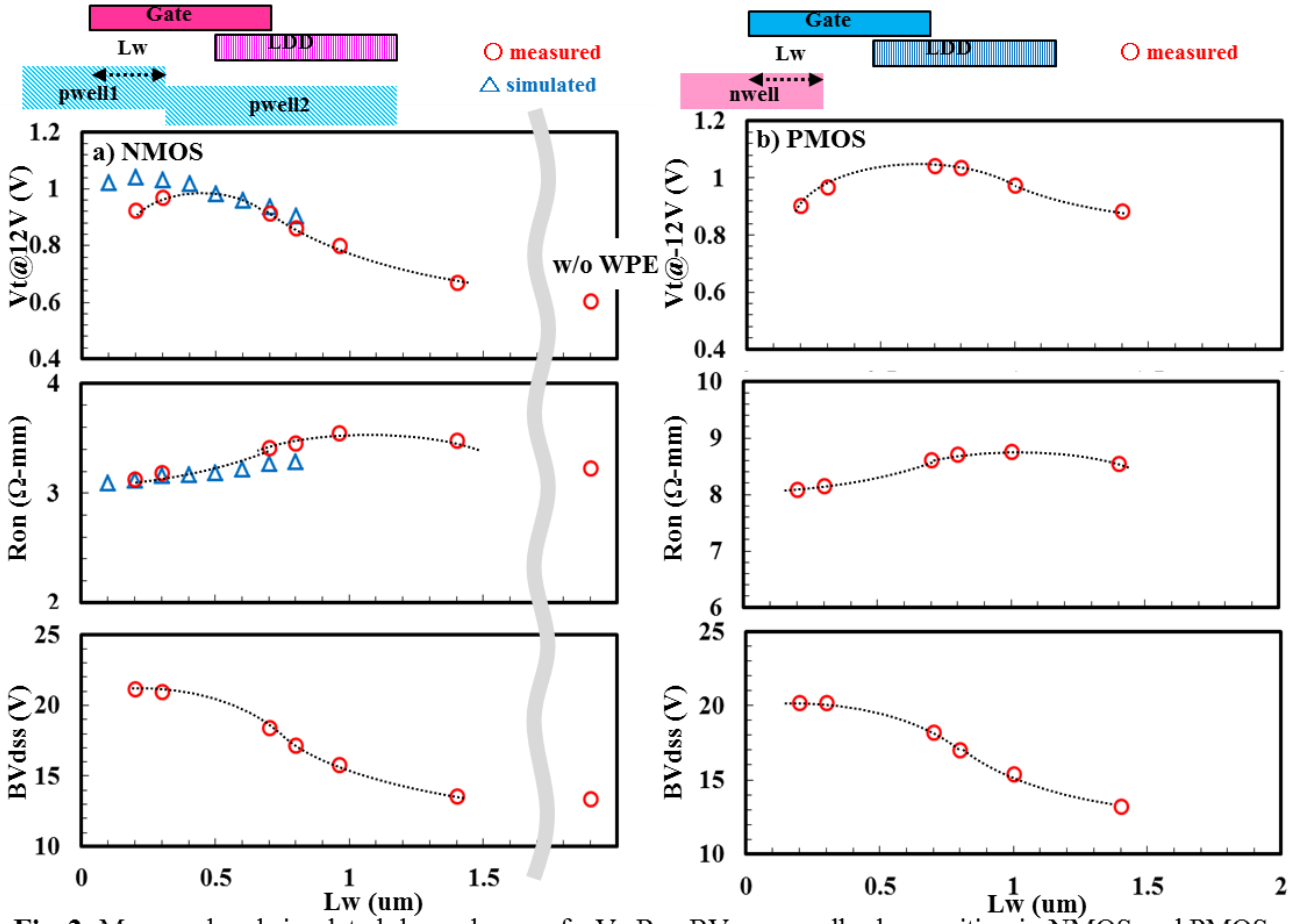

Fig. 2: Measured and simulated dependence of a V_t, R_{on}, BV_{dss} on well edge position in NMOS and PMOS.

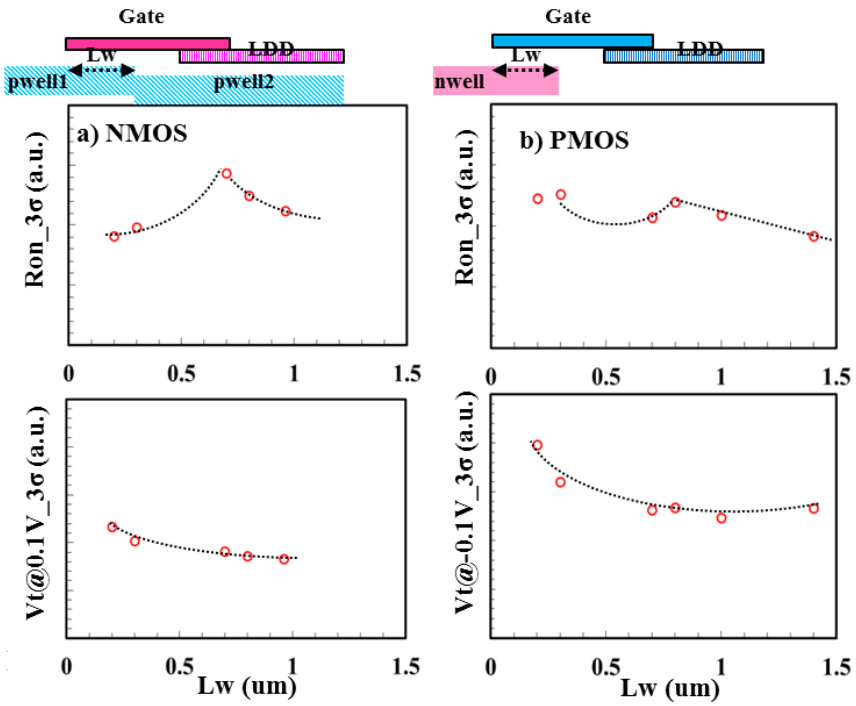

Fig. 3: Measured 3σ of R_{on} in a wafer.

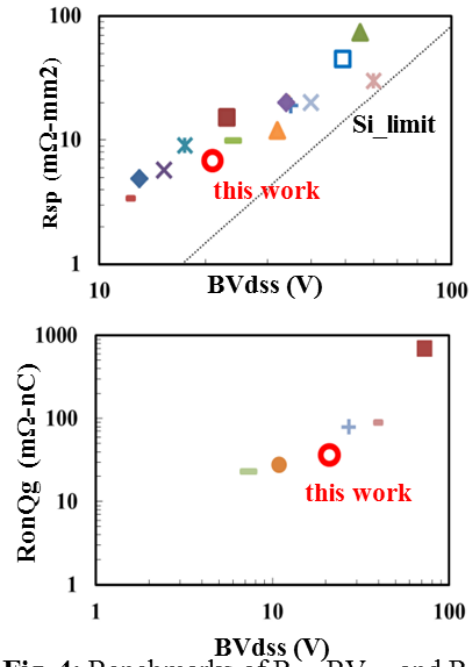

Fig. 4: Benchmarks of R_{sp}- BV_{dss} and $R_{on}Q_g$- BV_{dss} of lateral NMOSs.