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Impact of the silicon on diamond structure for high temperature switching applications

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Abstract

This paper evaluates Silicon-on-diamond (SOD) structure compared to the conventional SOI for high temperature switching applications. For high temperature applications (> 473 K), major loss is due to on-resistance and leakage current. The power MOSFETs fabricated on SOD substrate shows lower loss compared with that fabricated on the conventional SOI substrate.

1. Introduction

High temperature applications of the power ICs and power devices have attracted attention because of increasing the demand for automotive, jet engine for aircraft, space exploration[1]. Silicon on insulator (SOI) technology is attractive for these applications [2] because of lower leakage currents as well as high reliability (immunity of temperature induced latch up). Thin-film approaches are promising because it showed quite lower leakage current[3]. When the SOI power MOSFETs operate at high temperature, on-resistance and leakage current increase because of self-heating effect due to poor thermal conductivity of SiO_2[3]. Silicon on diamond substrate (SOD), which uses diamond film used as an insulator film, is attractive because the thermal conductivity of diamond film is much higher than that of SiO_2[4]. The higher thermal conductivity diamond film reduces the temperature of active Si layer [5] and this suppresses the increase in leakage current and on-resistance caused by self-heating effect.

This paper reports the impact of the SOD structure for high temperature switching applications based on experimental results and 2-D device simulations.

2. Device structure and Fabrication process.

The schematic cross section of the fabricated and simulated thin-film SOI power MOSFET Figs. 1(a) and a circuit diagram for switching operation is shown in Figs. 1(b). The main structural parameters are listed in Table 1 and a material constant used in simulations are listed in Table 2. The thermal conductivity of diamond film is assumed to 20 W/m/K, which is the thermal conductivity of nano-crystalline diamond formed by plasma CVD[4]. We used SiO_2 and diamond films for a buried insulator. The thickness of the insulator was set by consideration of target breakdown voltage (in this case 30 V).

Table.1 The main structural parameters.

Top Si layer (μm)	0.14
Buried oxide (μm)	0.4
Gate oxide (nm)	20
Channel Length (μm)	1.5
Gate width (μm)	20
Drift Length (μm)	1.5
Impurity concentration in drain offset region (cm-3)	1.7×10^{17}

Table.2 Material constants used in simulations

Parameter	Si	SiO2	Diamond	Air
Specific heat [J/kg/K]	700	780	520	1000
Density[kg/m³]	2330	2200	3500	1.2
Thermal Conductivity [W/m/K]	145	1.4	20	0.026

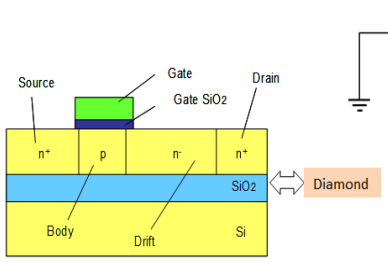

Fig.1(a)

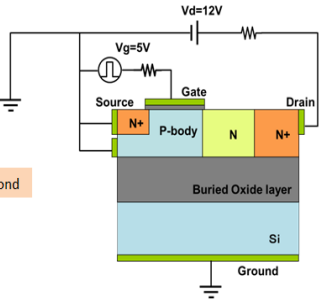

Fig.1(b)

Fig.1(a) Schematic cross section and (b)the circuit diagram used for 2-D device simulations.

3. Result & Discussion

Dependence of the leakage current and on-resistance on temperature at gate width of 100 cm is shown in Fig. 2. The

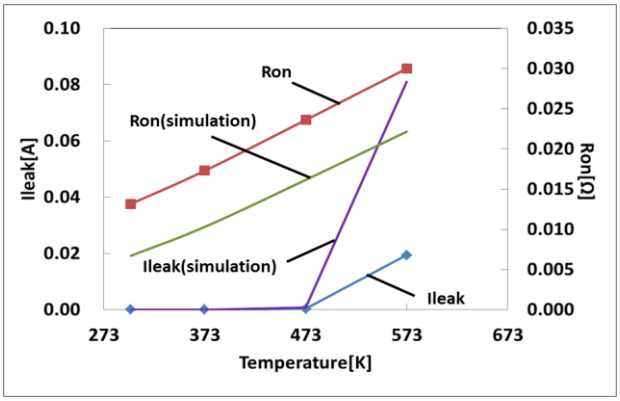

Fig. 2 Dependency of leakage current and on- esistance on temperature.

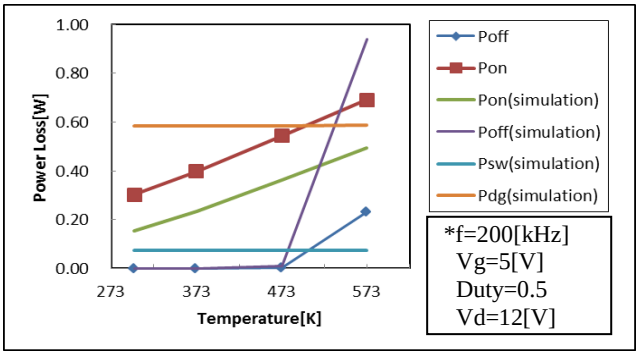

Fig. 3 Dependence of power Loss of SOI power MOSFET on temperature.

leakage current and on-resistance increase with increasing temperature. Especially, leakage current steep increases when temperature is more than 473 K.

Dependence of loss on temperature obtained by 2-D device simulation are shown in Fig. 3. The total gate width is the same as Fig. 2. The conduction loss and loss caused by leakage current obtained by experimental results are also shown in this figure. The power loss was calculated by the following;

$$P = P_{sw} + P_{on} + P_{off} + P_{dg}$$
$$= \frac{I_{swon} V_{swoff}}{6} (\triangle T_{on} + \triangle T_{off}) f_{sw} +$$
$$DI^2_{swon} R_{on} + (1\text{-}D) I_{swoff} V_{swoff} + Q_G V_G f_{sw} \ [W] \quad (1)$$

P_{sw}: Switching loss, P_{on}: Conduction loss,
P_{off}: Loss caused by leakage current
P_{dg}: The charge-and-discharge loss of gate oxide
I_{swon}: on current, V_{swoff} : V_d, ΔTon :on time,ΔT_{off}: off time,
f_{sw} :switching frequency, Ron: on-resistance, D : Duty ratio,
Q_G : Gate charge

P_{sw} and P_{dg} is almost constant regardless of temperature. P_{on} and P_{off} increase with increasing temperature. Thus, total loss increases with increasing temperature.

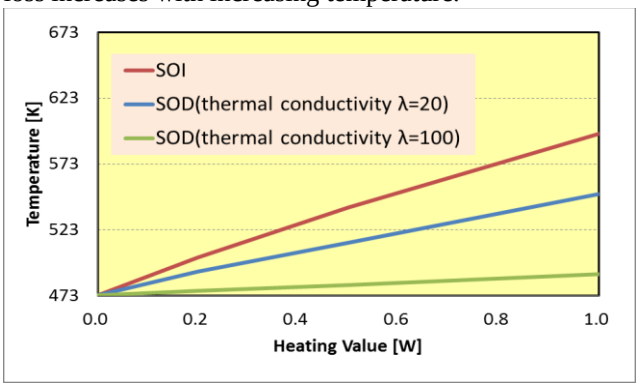

Fig. 4 Dependece of tempareture on power loss.

Dependence of temperature of active Si layer on power loss at environmental temperature of 473K is shown in Fig. 4. When we calculate temperature of active Si layer, we use following equation;

$$\rho c \frac{\partial T}{\partial t} = \frac{\partial}{\partial x}(\lambda \frac{\partial T}{\partial x}) + \frac{\partial}{\partial y}(\lambda \frac{\partial T}{\partial y}) + Q_v \quad (2)[6]$$

ρ: Density , c: specific heat capacity , T: temperature,
t: time, λ: thermal conductivity, Qv: heat generation density.

Temperature of active Si layer is raised by power loss and increases with increasing power loss. Temperature of active Si layer for SOD is lower than that for SOI. The reduction in temperature of SOD compered to the conventional SOI structure is 46K at power loss of 1 W when the thermal conductivity of diamond film is even at 20 W/m/K.

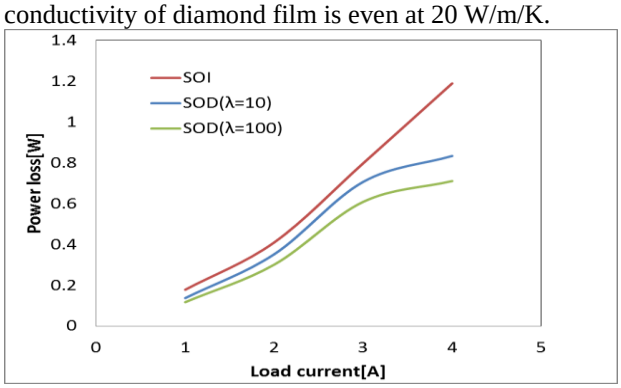

Fig. 5 Dependence of power loss on load current.

Dependence of power loss on load current at environmental temperature of 473K is shown in Fig. 5. When we estimate power loss, we take into consideration of self-heating effect. The loss is steady state and steady state temperature is obtained by results of Fig. 4. In this figure, we calculate P_{on} and P_{off} using experimental date. The power losses of the power MOSFET fabricated on SOI, SOD (λ: 20W/m/K), and SOD (λ: 100W/m/K) at load current of 4 A are 1.2 W, 0.83 W, and 0.71W, respectively. The power loss for SOD substrate is lower than that for the conventional SOI substrate because SOD can suppress the self-heating effect and this reduces P_{on} and P_{off}.

4. Conclusions

We evaluate the loss for high temperature switching. The conduction loss and loss caused by leakage current increase with increasing temperature. Especially loss caused by leakage current steeply increases when temperature is more than 473 K. On the other hand, switching loss and the charge and discharge loss of gate oxide is almost constant regardless of temperature. SOD structure suppressed the self-heating effect and reduces the loss caused by self-heating effect.

References

[1] C. Buttay, D. Planson, B. Allard, D. Bergogne, P. Bevilacqua, C. Joubert, M. Lazar, C. Martin, H. Morel, D. Tournier, and C. Raynaud, Mater. Sci. Eng. B, 176, 283 (2011) .
[2] H. Tomida, H. Eguchi, S. Kijima, N. Honda, T. Yamada, H. Yamawaki, H. Aoki and K. Hamada. Proc. of ISPSD'2011, p.28, 2011.
[3] Y. Morisawa, T. Kodama, and S. Matsumoto: Microelectron. Reliab. 52, 2380 (2012).
[4] K. Tsugawa, M. Ishihara, J. Kim, Y. Koga, and M. Hasegawa:Phys. Rev. B82, 125460,(2010)
[5] K. Nakagawa, T. Kodama, S. Matsumoto, T. Yamada, M. Hasegawa, and S. Nishizawa, in Ext. Abs. SSDM2013, p.1044, 2013.
[6] Y. Iwai, T. Oomura, Y. Koito, K. Kobayashi, T Tomura, M. Haneda, S. Hirasawa, H. Yoshida: Netsuryuutai no simulation (2010) [in Japanese]