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Simulation analysis of the potential causes for the low J_{sc} in GaAsN solar cells

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Abstract

To investigate the origin of the low J_{sc} in GaAsN single-junction solar cells, SCAPS software is introduced to simulate the evolution of J_{sc} with the adjustment in front-part region of n^+-p GaAsN configuration (n^+-GaAs/n^+-GaAsN interface states, cap layer thickness, emitter thickness). The results show that the existence of interface states can induce the formation of a sink for holes, which can cause a deterioration of the J_{sc}. In addition, the optimized thickness of cap layer and emitter is important for the recovery of J_{sc} value, i.e., 10nm and 70nm, respectively. Finally, an above 15% conversion efficiency is expected with a 25mA/cm^2 J_{sc} value.

1. Introduction

III-V multi-junction solar cells have the potential to achieve a high solar energy conversion efficiencies exceeding 40%, and are very attractive for both space and terrestrial applications[1]. (In)GaAsN, with a band gap energy of 1.04eV, is confirmed to be an very promising candidate for the third sub-cells, not only because of its optimal bandgap but also its almost the same lattice constant as GaAs or Ge substrate[2]. However, the reported J_{sc} in (In)GaAsN single-junction solar cells is too small to meet the expected requirement. It has been proved that a 17mA/cm^2 J_{sc} under a GaAs filter at 1-sun under AM0 conditions need to be obtained to realize the current-matching. In this contribution, simulation analysis is carried on to explore the possible causes that make the J_{sc} decrease.

2. Experimental procedure

n^+-p type GaAsN homojunction solar cells configuration is introduced in simulation and real experiments. Fig. 1 shows the corresponding schematic diagram consisting of cap layer n^+-GaAs, n^+-GaAsN emitter, p^+-GaAsN base layer and a heavily doped p-GaAs substrates. The corresponding bandgap and doping level for cap layer, emitter and base are fixed at 1.26eV, 1.26eV and 1.42eV and 2×10^{18}cm^{-3}, 3×10^{17}cm^{-3} and 1×10^{16}cm^{-3}. SCAPS software was used to simulate the evolution of J_{sc}. In this contribution, density of interface states, thickness of cap layer and emitter is set as input parameters.

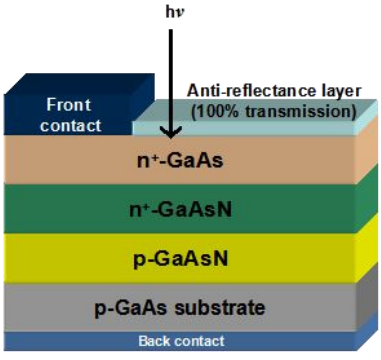

Fig. 1 GaAsN single-junction configuration for simulation

3. Results and discussion

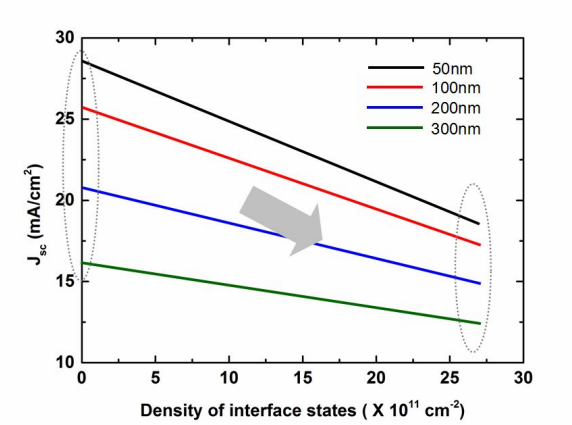

Fig. 2 J_{sc} vs. density of n^+-GaAs/n^+-GaAsN interface states with different thickness of emitter

n^+-GaAs/n^+-GaAsN surface vs. J_{sc}

Generally, a substantial portion of incident short-wavelength photons will be absorbed in emitter layers because of its high absorber coefficient in GaAsN material. If a great deal of n^+-GaAs/n^+-GaAsN interface states exist, a sink for holes generated in the emitter will be formed. Fig. 2 shows the changes of J_{sc} as a function of the density of interface states with different thickness of emitter. It is clear that J_{sc} linearly decreases as the density of interface states increasing. In addition, at a fixed density of interface states, a decreasing thickness of emitter is beneficial for the recovery of J_{sc} value. As the emitter layer decreasing, more incident light will be absorbed in the base layer, thus decreasing the possibilities of recombination at the front surface. Also, it can be observed in Fig. 2 that in large density of interface states region, the influence of the thickness of emitter layer on J_{sc} is relatively small. Fig. 3 exhibits the current depth distribution (electron current, hole current, total current) with and without interface states, the thickness of cap and emitter layer are fixed at 60nm and 100nm, respectively. when the interface states exist, it is

clear that a steep sink for holes is formed at the front surface.

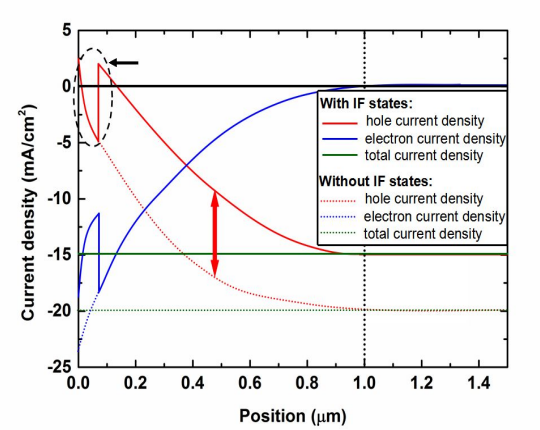

Fig. 3 Current depth distribution (electron, hole, total) with/ without interface states (the thickness of cap and emitter layer are fixed at 60nm and 100nm)

n^+-GaAsN emitter vs. J_{sc}

Fig. 4 shows the changes of J_{sc} as a function of the thickness of emitter with different thickness of cap layer. Two region can be separated: when the thickness of emitter is above 70nm, a slightly increase in J_{sc} that does occur with the decreasing thickness of emitter can be ascribed to a reduced bulk losses in the n^+-GaAsN emitter. when the thickness of emitter is below 80nm, the decrease in J_{sc} is caused by the loss of a few carriers generated at the distance close to the front surface. In addition, with a fixed thickness of emitter, the increasing thickness of the cap layer can induce a dramatically decreasing in J_{sc}.

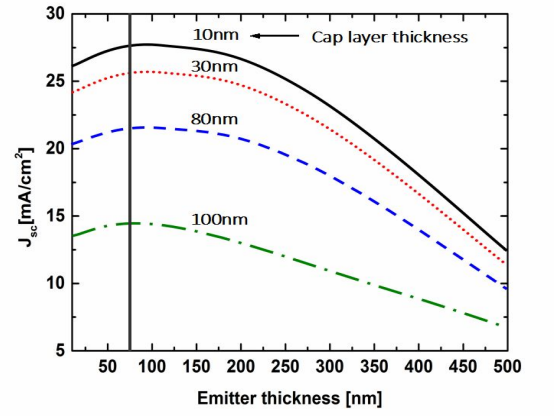

Fig. 4 J_{sc} vs. emitter thickness with different thickness of cap layer

In our lab, over 7% conversion efficiency of GaAsN single-junction solar cells has been achieved with a J_{sc} value only 15 mA/cm^2. Through setting some optimal parameters, i.e., emitter thickness~70nm, cap layer thickness~10nm, density of interface states<10^{12} cm^{-2}, lifetime~1ns (mainly be realized by the improved material quality of GaAsN-based layer with a decreasing in defects density), a 15% conversion efficiency can be reached with an J_{sc} value of 25mA/cm^2 (see Fig. 5).

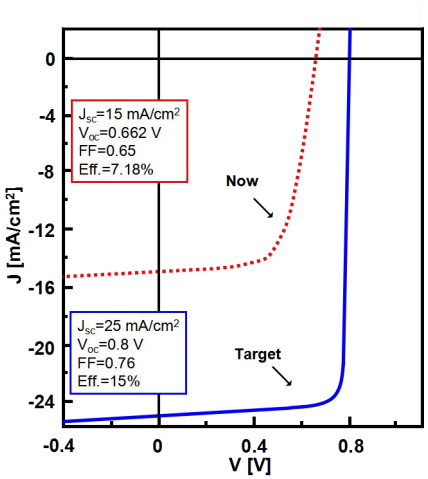

Fig. 5 *J-V* curve obtained in our lab. and the optimized *J-V* achieved by simulation

4. Conclusions

In summary, the numerical simulation results show that the existence of n^+-GaAs/n^+-GaAsN interface states can cause the J_{sc} deteriorate seriously by forming a sink for holes. In addition, an optimized thickness of cap layer and emitter is set to be 10nm and 70nm, respectively. Finally, an above 15% conversion efficiency is expected with a J_{sc} value of 25mA/cm^2.

Acknowledgements

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References

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