Ultra-low reflective micro-structures fabricated by one-step advanced silicon etching on silicon surface

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Abstract

In this paper, a one-step method to fabricate nano-micro structures was reported. This novel method was completely compatible with the traditional process and would not introduce any contamination ions. The specific etching system for this method was a standard surface technology system (STS) with a phase-delay producer. The formation and evolution mechanism for these structures were investigated and specific experiments were carried out to verify the relationship between structures scale and process parameter. At last, the reflectance was measured, only 0.9% proving that this method was very promising for the optical application.

1. Introduction

Nowadays, with the rapid development of the optoelectronic industry, there is a growing demand for large-scale silicon surface modification and direct optoelectronic integration. The traditional silicon surface modification methods include femtosecond laser pulses, metal-assisted wet etching and deep reactive ion etching (DRIE). The femtosecond laser pulses could hardly be adopted for the industrial production. The metal-assisted wet etching would bring in the metal contamination, which would be fatal for the integration. And the traditional reactive ion etching is usually conducted at extreme conditions, such as the low temperature. Thus, in this paper, a mild and complete compatible surface modification is reported and the physical mechanism is studied. Then the specific experiments and practical surface reflectance measurement were carried out, proving its potential in the optical application.

2. Mechanism and experiment

In a standard STS-ICP etching system, the bias voltage is the key factor determining the ions impacting energy and flux density to the substrate surface. Just as the figure. 1(a) shows, when the bias is supplied at a continuous low voltage, the ions would gain low energy through the plasma sheath. Then the ions energy would be further dispersed to a lower extent after the trench travel filled with collisions with the neutral radicals. When the etching process progresses to some degree that the trench travel is sufficient to disperse the most ions energy, few ions would impact and sputter the sample surface that it is not enough to occupy the whole surface at one instant. This leads to a non-uniform etching overall the surface, while as depicted in figure. 1(b), at the next constant the left blank space, if the bias is still biased by a low voltage, would have much more chance to receive another non-uniform etching due to the height difference, known as the shadow effect. Thus under this condition the non-uniformity would not accumulate. This could explain why in the previous study, Nguyen's experiment, the structures scale could only vary in the range of 1 to 2 µm by adjusting the bias voltage [1]. However, if the bias voltage is switched from low level to high lever after one non-uniform etching, the situation would be much more different. As the figure. 1(c) and figure. 1(d) shows, the most ions would gain sufficient energy to overcome the trench dispersion to reach the substrate. And for the reason that the ions are at high energy level, the reflect effect is dominant, which means the ions would be reflected from the peak and the trough would receive more ions [2]. Thus the non-uniformity would accumulate and the sharp roughness could form.



Fig. 1 The mechanism of physical evolution.

The figure. 2 is the Monte Carlo (MC) simulation result about energy distribution of ions final reaching substrate. It is obvious that with the etching depth increasing the total numbers of ions arriving at the substrate (the area) would decrease and also at low level bias supply the total numbers of ions final impacting the substrate would be relatively smaller than that at low level.

To achieve the goal that the sequence etching cycle would undertake under different effective bias voltages, a standard STS-ICP etching system is connect with a delay producer just as figure .3 shows.

The practical experiments were conducted with the parameters shown in the Table I. To make sure that a stable electromagnetic environment was established, the sample 3 and sample 4 were both delayed after a whole period.



Fig. 2 The MC simulations about impacting ions energy distribution of different bias voltages under various etching depth.



Fig. 3 The scheme of the whole system.

The figure. 4 shows the surface morphologies of mc-Si for different etching conditions. It is very apparent to conclude that only as the bias voltage decrease to half with no delay, the sample surface would be little rougher, while the surface structures scale would sharply increase to micro-scale with certain delay just as figure. 5 shows.



Fig. 4 The SEM of the silicon surface. The image (a) – (d) shows samples with no delays and bias voltage at 100V, with no delays and bias voltage at 50V, with delays of 390° and bias voltage at 100V and with delays of 450° and bias voltage at 100V.

The figure. 6 shows the measured reflectance of the samples. It is well noted that after the disordered etching, the samples surface reflectance has a sharp decrease, re-

sulting from the growing micro-scale structure.



Fig. 6 The sectional SEM of the samples. Image (a) delays of 390° and bias voltage at 100V and image (b) delays of 450° and bias voltage at 100V.



Fig. 6 The surface reflectance of the samples.

Tabla I

Table 1 Experiment parameters			
Sample	Bias	Etching	The phase delay between upper
	voltage	time	and bias power (degree)
		(min)	
1	100	30	0
2	50	30	0
3	100	30	390
4	100	30	450

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3. Conclusions

This paper has introduced a novel method to fabricate micro-structures on the silicon surface. The investigation into the physical mechanism and the MC simulation has predicted its growth and to our best knowledge, the scale of the obtained surface structures through the practical experiments is largest. And the reflectance measurement has also indicated the great potential on optical application of this method.

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