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Joule Heating Induced Bonding Interface Improvement and Ti Breakthrough by Electron Bombardment for 40-μm Pitch of Cu TSV and Cu/Sn μ-Bump Pair

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1. Introduction

Since 3D integration is introduced into advanced semiconductor industry, the dimension of 10-μm diameter Cu TSV and 20-μm size Cu/Sn μ-bump pairs with the 40-μm pitch separation enabling thousands of vertical interconnects/cm^2 density has received large attention [1, 2]. In the recent papers or news, both Xilinx/tsmc by CoWoS^{TM} [1] and Qualcomm [2] use the dimension mentioned above of TSVs and pillar pairs to integrate 28-nm or 40-nm node chips together to achieve the high performance Virtex®-7 HT product and 4-die of wide-I/O memory with the JEDEC MPGA spec in stacking, respectively. For the dimension of 20-μm size Cu pillar Sn bump, bonding thickness smaller than 8-μm is used to reduce the Sn squeeze out and short circuit issues [4, 5]; however, this thickness close to 5-μm physical limitation of intrinsic Cu/Sn IMC growth makes a poor quality of bonding interface [3]. In general, although bonding area and yield can be inspected by SAM (Scanning Acoustic Microscope), the bonding interface behaviors cannot be directly detected by this equipment. As the results, in this work, the bonding interface behavior and grain formation evolution are investigated by comparisons of electrical measurement, FIB, SEM, and EDX inspections.

2. Experimental

The specifications of test structure include 10-μm Cu TSVs embedded in 40-μm thin silicon substrate, electro-plated 3-μm/2-μm-thick Cu/Sn bumps, and 50-nm Ti adhesion layer between SiO_2 and Cu metal tracer, as shown in Fig. 1. Fig. 2 shows the experimental procedure. The test structure is fabricated by a sequence process of Cu TSV formation, Cu/Sn micron-bump fabrication, 250 °C wafer bonding, backside thinning, and redistribution metal layer. The design includes daisy chain (N=200) and Kelvin patterns, which are electrically measured before and after the 6.36 x 10^4 A/cm^2 current stressing test for 100 hours and 2000's TCT (JESD22-A104B). Finally, the FIB/SEM images collocating with electrical measurement results are evaluated to characterize bonding interface behaviors.

3. Results and Discussion

Fig. 3 shows the cross-sectional SEM image of the test structure with the 10-μm Cu TSV, 20-μm bump size, and 40-μm pitch between two Cu TSV and bump pairs. The EDX/SEM results show that all Sn atoms are reacted with Cu to form Cu_3Sn ε-phase IMC, and lots of Cu_3Sn ε-IMC on both side surfaces are just contacted rather than totally merged together.

Interesting observations on grain evolution and joule heat induced resistance variation are worth mentioned. Fig. 4 (a)-(d) and Tab. 1 show the cross-sectional FIB ion images and daisy chain (N=200) resistance results of Cu TSV and Cu/Sn μ-bump pair during current stressing test and TCT, respectively. In Tab. 1, we find that daisy chain resistance improves as the increase of current stressing test duration, as well as the duration of TCT. The cross-sectional ion beam images give the clear clarification of species which kind of grain belongs to Cu TSV, Cu metal tracer and Cu_3Sn ε-IMC. Therefore, an imperfect bonding interface as test structure fabricated is found in Fig. 4(b), while no visible bonding interface can be detected after the 6.36 x 10^4 A/cm^2 DC current stressing in Fig. 4(c) and 2000's TCT in Fig. 4(d), respectively. The results imply that Cu_3Sn ε-IMC bonding interface can be removed through both temperature cycle from -55 to 125 °C and DC current, which induce joule heating. Finally, the daisy chain resistance can be hence improved.

Surprisingly, when we take a close look at the cross-sectional SEM image of the sample after 100 hour current stressing test, Ti adhesion between Cu tracer and Cu TSV is broken through the electron bombardment of current, as shown in Fig 5(a)-(c). Fig. 5(c) indicates the 1.1-μm Ti breakthrough width and its electron flow direction. In this case, Ti breakthrough does not result in circuit failure, and the resistance change might majorly come from bonding interface removal. However, in the case of Sn rich or a thin Cu metal tracer, due to the breakthrough of Ti layer, Cu_3Sn IMC might dissolve and diffuse into Cu TSV, resulting in a significant reliability issue.

4. Conclusions

In this work, joule heat induced bonding interface improvement and Ti breakthrough between TSV and Cu pillar are observed. For the 40-μm-pitch Cu TSV and Cu/Sn μ-bump, a bonding thickness smaller than 8-μm is used to reduce squeezing out issue, but it might make imperfect bonding interface. This imperfect bonding interface can be improved after multiple circuit operation and the break-

through of Ti layer does not present a real circuit damage in the current Cu/Sn dimension.

Acknowledgements

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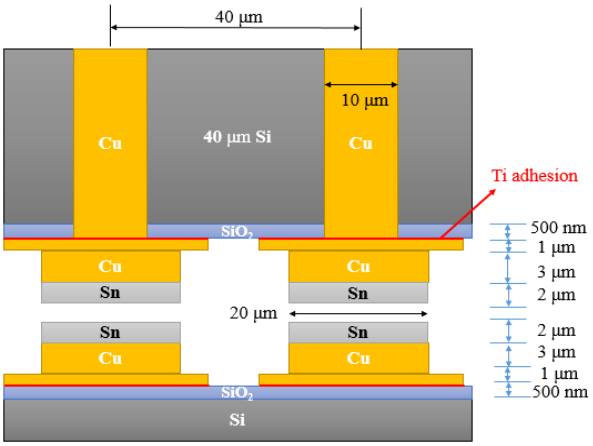

FIG. 1 Schematic diagram of test structure with 10-μm Cu TSV, 20-μm Cu/Sn μ-bump size, 40-μm pitch…etc.

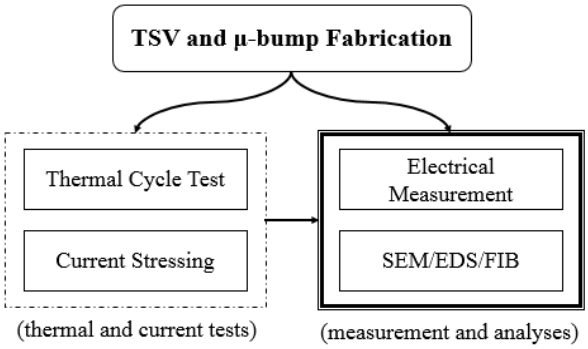

FIG. 2 Experimental procedure of the study including fabrication, two simple reliability tests and several analyses.

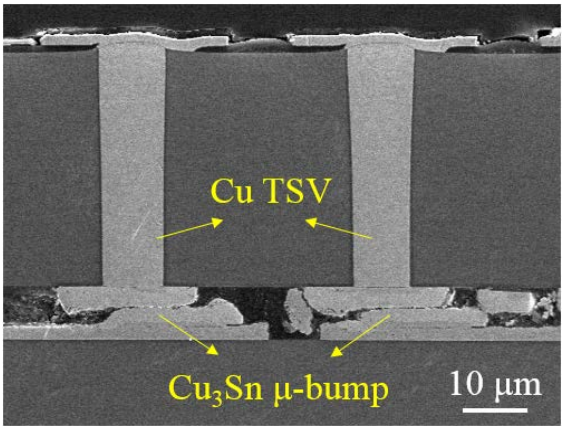

FIG. 3 Cross-sectional SEM image right after the test structure successfully fabricated.

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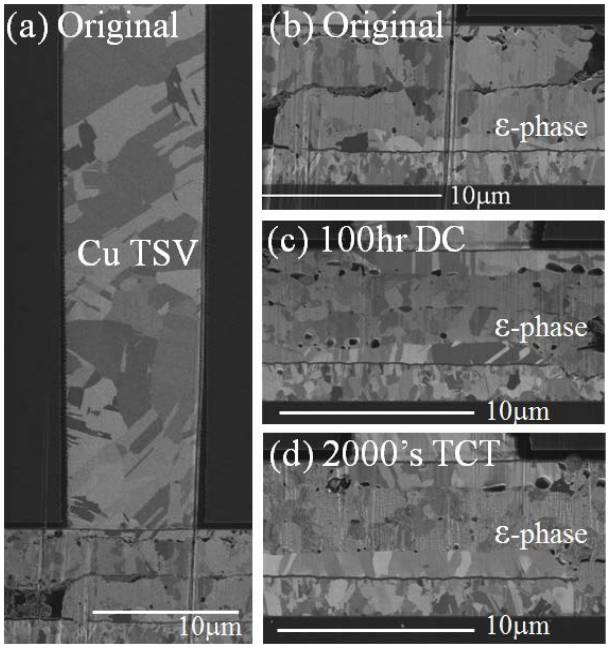

FIG. 4 Cross-sectional FIB ion images of (a)-(b) original sample and (c) after current stressing test, and (d) 2000 times of TCT. A clear grain evolution can be observed within these figures.

Table 1 Daisy chain (N=200) resistance evolution during TCT and DC current stressing

Thermal cycle test, JESD22-A104B, -55 to 125 °C		
Original	1000's cycle	2000's cycle
5.23 Ω	5.14 Ω	5.1 Ω
Current stressing test, 6.36 x 10^4 A/cm^2 for 100 hours		
Original	50 hours	100 hours
5.173 Ω	5.142 Ω	5.107 Ω

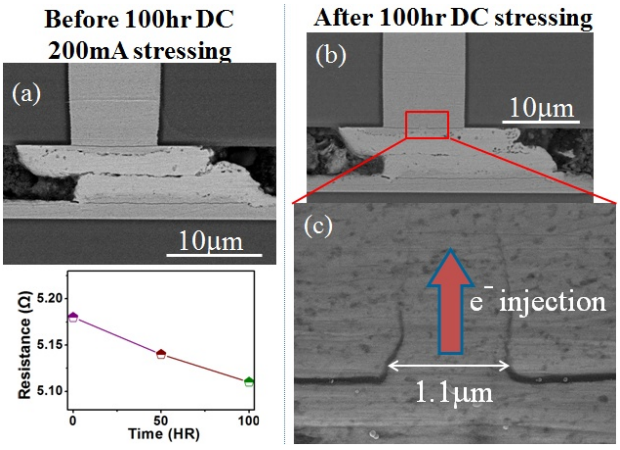

FIG. 5 Cross-sectional SEM image of evidence of Ti breakthrough.