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Extraction of Source/Drain Series Resistance Components Optimized for Double-gate FinFETs

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Abstract

Source/Drain series resistance (R_{sd}) is extracted using methods applicable to short channel n- and p-type FinFETs. R_{sd} is decomposed into spreading, sheet, and contact resistances using the analytic model considering top and sidewall contact resistivity separately. Resistivity parameters in the analytic model were effectively extracted from experimental data, and the R_{sd} components with different fin widths were investigated.

1. Introduction

Fin field effect transistors (FinFETs) have gate controllability and immunity from short channel effects, but suffer from increased source/drain (S/D) series resistances (R_{sd}) [1]. Analytic models for R_{sd} of FinFETs with double-gate [2] and polygonal epitaxy [3] have been developed, and geometrical effects on R_{sd} are investigated using 3-D device simulations. However, the adoption of the analytic models to the experimental data is lacking.

In this paper, we extracted R_{sd} of both n-type and p-type double-gate FinFETs using the method applicable to each short channel devices separately [4-5]. Resistivity parameters in the analytic models were extracted using the R_{sd} values of FinFETs with different fin widths (W_{fin}) and spacer lengths (L_{sp}).

2. Experiments

<110> FinFETs were fabricated on a single SOI wafer. After the Si fins were patterned using a nitride hard mask, H_2 annealing was performed to reduce surface roughness effects. Hafnium high-k material with a thickness of 2 nm was formed by atomic layer deposition, followed by chemical vapor deposition of 10-nm TiN and 250-nm poly Si. After gate etching and nitride spacer formation, the source and drain regions were pre-cleaned with HF and silicided to form NiSi. Geometrical parameters of FinFETs are shown in Table I.

R_{sd} values were extracted from each 10 devices at gate voltage (V_{GS}) of 1.5 V using the approach of [4].

3. Results and Discussion

R_{sd} of FinFETs is decomposed into spreading (R_{sp}), sheet (R_{sh}), and contact resistances (R_{con}) (Fig. 1). Analytic models of R_{sp} and R_{sh} are equivalent to eqs. (1) and (4) in [3] excluding R_{sp} at the top channel. R_{con} is modeled using transmission line model [6], but the contact resistivity between sidewall and top surfaces are considered separately due to different surface orientations for <110> FinFETs. Analytic models of R_{sd} applicable to double-gate FinFETs are shown in Table II, where ρ_{ext} is the resistivity of S/D extension, $\rho_{int(side)}$ and $\rho_{int(top)}$ are the contact resistivity at sidewall and top silicon-to-silicide interfaces, respectively.

R_{sd} of n- and p-type FinFETs were extracted successfully (Fig. 2). n-type FinFETs had lower R_{sd} values than did p-type FinFETs, but both of them have similar DC performance degradation (87 %) affected by R_{sd} effects (Fig. 3).

Drain currents (I_{ds}) normalized to $2H_{fin}\cdot N_{fin}$ with and without R_{sd} effects are shown in Fig. 4. Normalized I_{ds} without R_{sd} are independent of W_{fin}, which implies that R_{sd} components, which are all dependent on W_{fin}, were extracted and eliminated from measured I_{ds} effectively.

Resistivity parameters were extracted as follows. Since FinFETs with different L_{sp} have same R_{con} and R_{sp} values (see (1), (3), (4) in Table II), ρ_{ext} can be extracted from the difference between R_{sd} values of the devices. $\rho_{int(side)}$ and $\rho_{int(top)}$ are then extracted using the R_{sd} values of the devices with different W_{fin}. As shown in Fig. 5, analytic models of R_{sd} for both n- and p-type FinFETs were fitted well to the experimental data.

Resistivity parameters were extracted with reasonable values similar as in [2-3] (Table III). p-type FinFETs had higher resistivity values than did n-type devices due to larger R_{sd} for all W_{fin} and L_{sp} splits. Both n- and p-type FinFETs have lower $\rho_{int(top)}$ than $\rho_{int(side)}$ because the silicide process is not performed well at the sidewall than at the top of the fins.

Using extracted resistivity parameters, R_{sd} components with different W_{fin} are calculated (Fig. 6). R_{con} is dominant for n- and p-type FinFETs with all different W_{fin}, and p-type FinFETs have larger R_{sd} values due to larger R_{con} mostly.

4. Conclusion

R_{sd} of n- and p-type FinFETs are extracted successfully using the model applicable to short channel devices. Resistivity parameters in the analytic models are extracted, and both FinFETs have lower $\rho_{int(top)}$ than $\rho_{int(side)}$. Therefore, fabricating FinFETs with larger top silicide surfaces such as epi-Si and tapered structure is promised to reduce R_{sd} values.

References

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Table I. Geometrical parameters of n- and p-type FinFETs.

Parameters	Values
L_g	40 nm
L_{sd}	75 nm
S_{fin}	200 nm
H_{fin}	40 nm
N_{fin}	20
W_{fin}	20, 30, 40, 60, 80 nm
L_{sp}	25, 125 nm (only for W_{fin} = 30 nm)

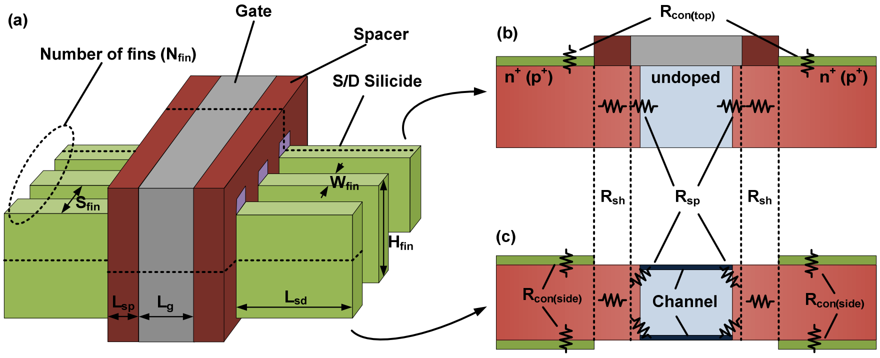

Fig. 1. Schematic diagram of (a) FinFET and (b) side-view and (c) top-view of FinFETs denoting source/drain series resistance (R_{sd}) components.

Table II. Analytic models of R_{sd} components optimized for FinFETs.

R_{sd} components	Equations
R_{sp}	$\frac{2\rho_{ext}}{\pi\cdot H_{fin}}\ln\left(\frac{3}{4}\cdot\frac{W_{fin}}{2x_c}\right)$ (1)
R_{sh}	$\rho_{ext}\times\frac{L_{sp}}{H_{fin}\times W_{fin}}$ (2)
$R_{con(side)}$	$\sqrt{\frac{\rho_{ext}\cdot\rho_{int(side)}}{W_{fin}\cdot H_{fin}^2}}\cdot\coth\left(L_{sd}\sqrt{\frac{\rho_{ext}}{W_{fin}\cdot\rho_{int(side)}}}\right)$ (3)
$R_{con(top)}$	$\sqrt{\frac{\rho_{ext}\cdot\rho_{int(top)}}{H_{fin}\cdot W_{fin}^2}}\cdot\coth\left(L_{sd}\sqrt{\frac{\rho_{ext}}{H_{fin}\cdot\rho_{int(top)}}}\right)$ (4)
R_{con}	$\left(\left(\frac{R_{con(side)}}{2}\right)^{-1}+\left(R_{con(top)}\right)^{-1}\right)^{-1}$ (5)
R_{sd}	$2\left(\frac{R_{sp}}{2}+R_{sh}+R_{con}\right)$ (6)

* x_c is the channel layer thickness, assumed to be 1 nm.

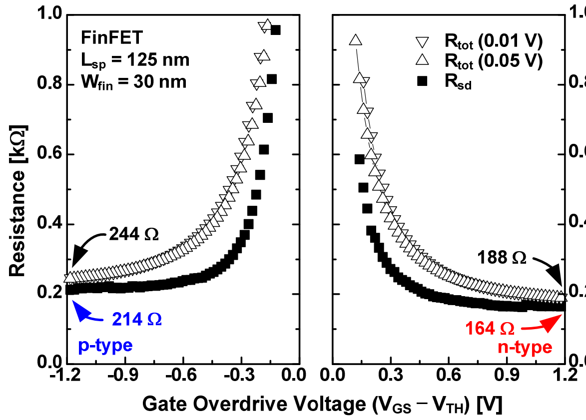

Fig. 2. Total resistance ($R_{tot} = V_{DS}/I_{ds}$) and R_{sd} values as a function of gate overdrive voltage. R_{sd} values were extracted at V_{GS} of 1.5 V at V_{DS} of 0.01 and 0.05 V for both n- and p-type FinFETs.

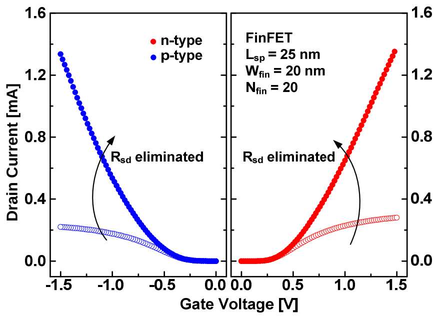

Fig. 3. Measured drain currents (I_{ds}) and I_{ds} after R_{sd} effect is eliminated for n- and p-type FinFETs at V_{DS} of 0.05 V.

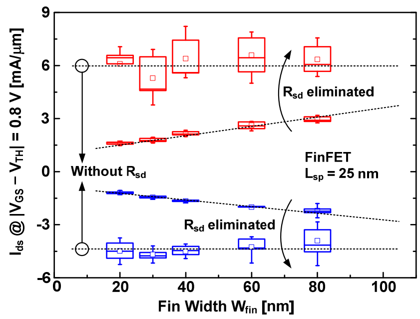

Fig. 4. Measured I_{ds} with and without R_{sd} normalized to $2H_{fin}\cdot N_{fin}$ for FinFETs with different W_{fin} at V_{DS} of 0.05 V.

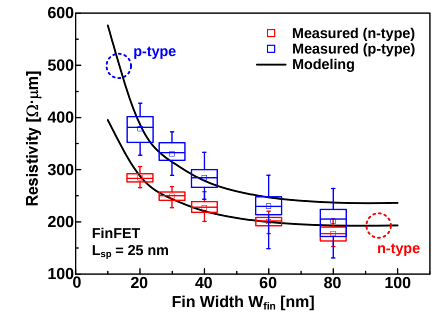

Fig. 5. Measured (symbols) and modeled (lines) resistivity (= $R_{sd}\cdot(2H_{fin}+W_{fin})\cdot N_{fin}$) of n- and p-type FinFETs with various W_{fin}.

Table III. Extracted resistivity parameters for n- and p-type FinFETs.

Parameters	n-type	p-type
ρ_{ext} [Ω·cm]	$6.53\cdot10^{-4}$	$8.35\cdot10^{-4}$
$\rho_{int(side)}$ [Ω·cm^2]	$1.97\cdot10^{-7}$	$4.69\cdot10^{-7}$
$\rho_{int(top)}$ [Ω·cm^2]	$2.25\cdot10^{-8}$	$2.48\cdot10^{-8}$

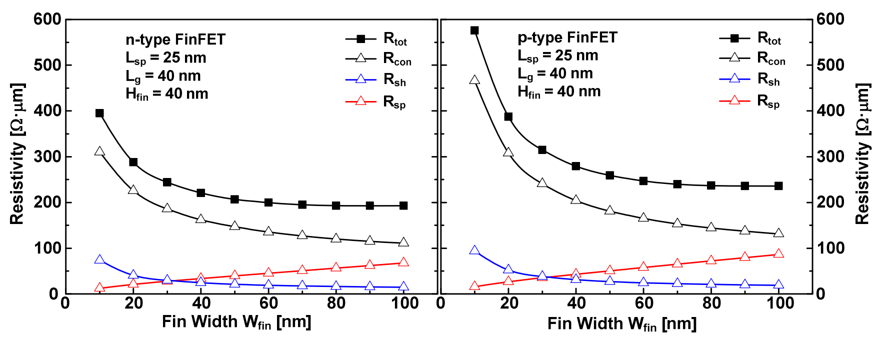

Fig. 6. R_{sd} components calculated using extracted resistivity parameters in Table III. R_{con} is dominant to R_{sd} for both n- and p-type FinFETs.