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New Concept of Planar Germanium MOSFET with Stacked Germanide Layers at Source/Drain

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Abstract

Novel Schottky barrier Ge-based MOSFET structure is proposed and simulated. The Source/Drain region is consisted with two stacked layers of germanide materials. The barrier heights of the top and bottom layer are different. The working mechanism and performance of the device is studied. The results show that ON-state current, leakage current, and transfer characteristics have been enhanced with the proposed structure. Besides, the requirement of GOI structures for leakage immunization can be released.

1. Introduction

In recent years, Ge-based MOSFETs have become one promising candidate for future device structure, which is due to the outstanding field effect mobility and drivability. Simultaneously, Ge-based device also suffers from the large leakage current. And germanium on insulator (GeOI) substrate and ultra thin germanium channel layer on SOI substrate are then fabricated to immunize the leakage current. For the real applicant, it's more difficult to fabricate GOI substrate than SOI case, because of the involved epitaxial procedure and defect density control [1-4].

Considering the source/drain of Ge device is always consistent of germanide material, due to the thermal budget requirement, herein, we propose to apply dual germanide layers at source/drain (DL-T). The performance of both *n*- and *p*-type DL-Ts are simulated with Sentaurus TCAD tools. It's found DL-T structure can improve the device performance and suppress leakage current effectively and the requirement of Ge film thickness can be greatly relaxed and even bulk Ge substrate can be applied to achieve low leakage current.

2. Device structure and working mechanism

The schematic structures of DL-T and conventional Schottky germanium MOSFET (SL-T) are illustrated in *Fig*.1. The performance of the two structures are then simulated and analyzed. *Table* 1 shows the major parameters and default values used in the device simulations. The tunneling mass and mobility models of Ge material [5] are set according to the calibration, which is well-fitting to the experimental data [6], as shown in *Fig*.2.

To explain the working principles of DL-T, the electrostatic potential distributions for *n*-type DL-Ts are illustrated in *Fig*.3. We can see the dual germanide layers form different barrier heights with germanium channel: the barrier height of the top contact near the surface (SBH_{te}= 0.05eV) is lower, and the barrier height of the bottom contact (SBH_{be}=0.38eV) is higher. In *Fig*.3(a), the electrostatic potential change rate is the highest in the source side of top germanium, which provides the main portion of ON-state current. In *Fig*.3(b), the change rate is nearly equal in the deep portion of source and drain side, due to the similar *SBH* for electrons and holes. In *Fig*.4, we show the OFF- and ON-state electron current density for both DL-T and SL-T. We can see DL-Ts shows apparent lower leakage current density at OFF-state. At ON-state, electron current density concentrates in the top barrier region and is basically the same in two structures. Then, DL-T can provide feasible way to design proper SBH_t and SBH_b to satisfy the drive ability and the leakage current requirement.

3. Performance estimation and discussion

Fig.5 shows the typical transfer curves of DL-T and SL-T (both with default values). For *n*-type device, the device drive ability can be enhanced by about two times: I_{on}=0.45mA/um for DL-T and 0.16mA/um for SL-T with 0.38eV electrons barrier (fix I_{off}=3uA/um) [5]. While the leakage current (represented by the valley value of I_{ds}, I_{min}) can be reduced by two orders of magnitude: I_{min}=0.43uA/um for DL-T and 0.26mA/um for SL-T with 0.05eV electrons barrier. Therefore, the DL-T can maintain the benefits of both low and high electron barriers.

After that, the gate work function is tuned to fit I_{off}=3uA/um. *Fig*.6 shows I_{on}, I_{min} with different SBH_b (fix SBH_t=0.05eV). It can be figured out that *n*-type DL-T with SBH_{be}=0.38eV has the smallest I_{min}. This phenomenon can be explained by the two type carrier conducing mechanism and a mid-gap energy level (0.66eV gap of germanium) can well suppress both electron and hole leakage current. And it can achieve the smallest I_{min} with SBH_{bh}=0.28eV for *p*-type case. *Fig*.7 plots the relationship between I_{on}, I_{min} and SBH_t, while applying the proper SBH_b. We can see lower SBH_t results in a larger current in electron current dominating region and both I_{on} and I_{min} increase while SBH_t becomes smaller. It's shown that the larger difference designed between SBH_b and SBH_t, the bigger I_{on}/I_{off} ratio we can obtain.

In *Fig*.8, the influences of the top germanide layer thickness (d_t) is studied with gate workfunction fixed. I_{on} shows nearly linear increase while I_{off} shows nearly exponential increase with d_t (increased from 1 to 15nm). It's noticed that, when d_t<5nm, I_{on} decreases faster, which implies the conducing current tends to locate near the surface region. In *Fig*.9, the thickness of Ge is changed from 10nm to 50nm, and d_b=d_{Ge}-d_t while d_t=3nm, We can see that bulk Ge and the increase of d_{Ge} will not induce much leakage current, which makes GeOI structure even not necessary to reduce the leakage current and the bulk structure promising for DL-Ts for its simplicity and cheapness in process.

4. Conclusions

We have proposed and simulated a novel DL-T structure. The results show that the DL-T exhibits better electrical properties than SL-T. The use of lower SBH_t improves the drive current while the higher SBH_b decreases leakage current. It's proved that the performance of planar Ge-channel device can be enhanced by applying DL-T structure.

References

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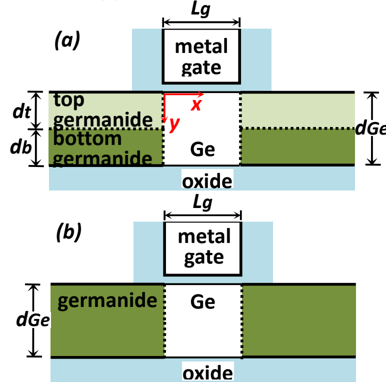

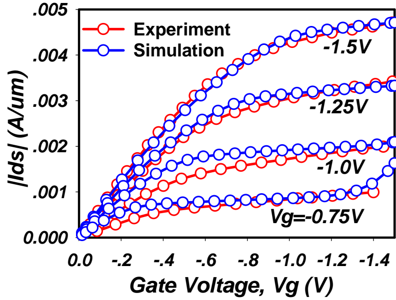

Fig.1 Schematic structure of (a) DL-T, (b) SL-T.

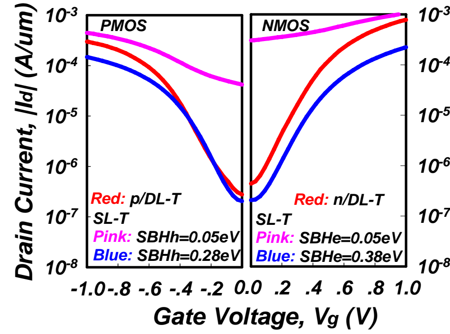

Fig.2 Simulation results calibrated with experimental data.

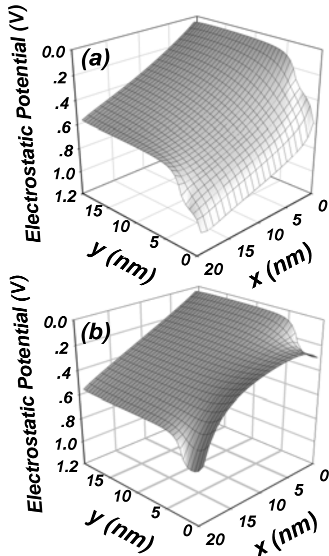

Fig.3 Electrostatic-potential distribution for DL-T: (a) ON-state, (b) OFF-state.

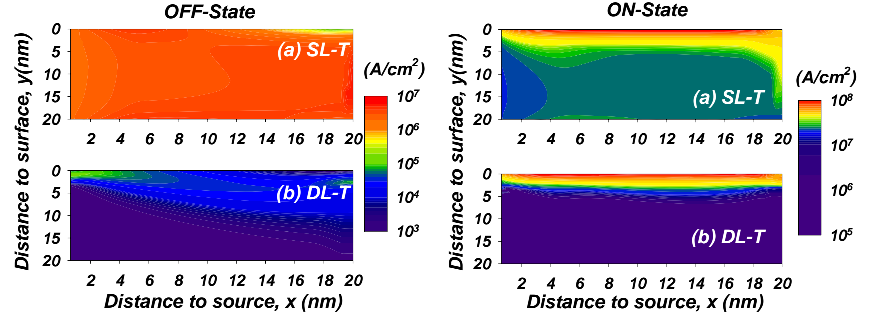

Fig.4 Electron current density distribution for *n*-type DL-T (with default values) and SL-T (*SBH*=0.05eV) at OFF-state and ON-state respectively.

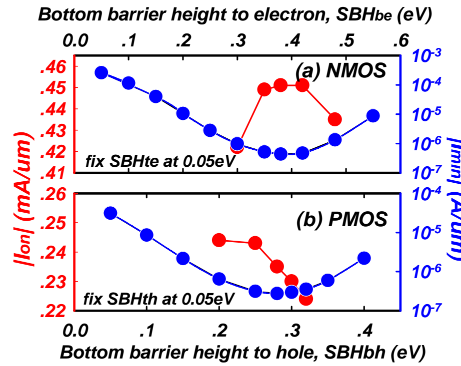

Fig.5 Transfer characteristics of DL-T (with default values) and SL-T.

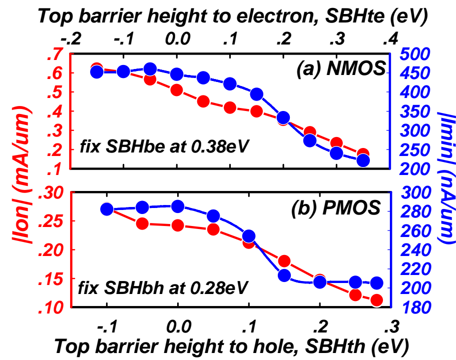

Fig.6 Ion (red line and symbols) and Imin (blue line and symbols) for DL-Ts with various *SBH*b. (a) NMOS and (b) PMOS. Ioff is fixed at 3uA/um.

Top barrier height to electron, SBHte (eV)

(a) NMOS
fix SBHbe at 0.38eV
(b) PMOS
fix SBHbh at 0.28eV
|Ion| (mA/um)
|Imin| (nA/um)
Top barrier height to hole, SBHth (eV)

Fig.7 Ion (red line and symbols) and Imin (blue line and symbols) for DL-Ts with various *SBH*t. (a) NMOS and (b) PMOS. Ioff is fixed at 3uA/um.

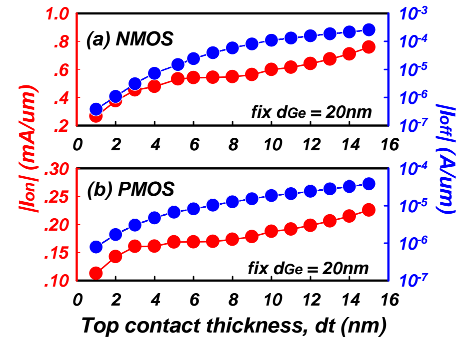

Fig.8 Ion (red line and symbols) and Ioff (blue line and symbols) for DL-Ts with various *d*t. (a) NMOS and (b) PMOS.

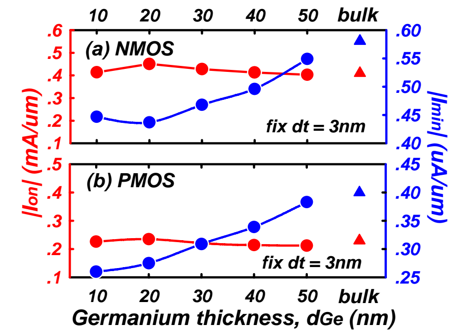

Fig.9 Ion (red line and symbols) and Imin (blue line and symbols) of DL-T with different germanium thickness *d*Ge and Bulk Ge. (a) NMOS and (b) PMOS.

Table 1. Simulations parameters

	Default
gate length (*Lg*)	20nm
Ge thickness (*d*Ge)	20nm
top germanide thickness (*d*t)	3nm
gate dielectric thickness (*T*ox)	1nm
bottom germanide thickness (*d*b)	*d*Ge-*d*t
n-type DL-T	
drain bias (*V*ds)	0.6V
gate bias (*V*gs)	1V
top barrier height to electron (*SBH*te)	0.05eV
bottom barrier height to electron (*SBH*be)	0.38eV
p-type DL-T	
drain bias (*V*ds)	-0.6V
gate bias (*V*gs)	-1V
top barrier height to hole (*SBH*th)	0.05eV
bottom barrier height to hole (*SBH*bh)	0.28eV
n-type SL-T/*p*-type SL-T	
source/drain barrier height (*SBH*)	0.05eV& 0.38eV