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Physical DC and Thermal Noise Models of 18nm DG Junctionless pMOSFETs

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Abstract

In this paper, we presented an improved dc model of scaled Double-Gate junctionless pMOSFETs that includes the field-dependent mobility and doping dependent diffusivity using a modified Einstein's relation for heavily doped semiconductors. The suggested new dc model was calibrated using the experimental results. Finally, we demonstrated, for the first time, a new noise model and their calculated results for channel thermal noise, induced gate noise, and their correlation noise as a function of biasing conditions, which provide physical insight of noise properties in 18nm Double-Gate junctinoless pMOSFETs.

1. Introduction

The double-gate (DG) junctionless (JL) MOSFET is one of the promising candidates beyond the 22-nm node due to its excellent gate controllability of the channel and the enhanced carrier-transport properties. Moreover without junctions between the source/drain and the channel, the fabrication process of DG JL MOSFETs is much easier and simpler. In previous researches, the dc characteristics and model of JL MOSFETs have been studied in [1, 2]. However, there has been no report about the thermal noise modeling of JL MOSFETs, which is critical in device operation.

In this paper, we present a new charge-based dc model and verify the new dc model using the experimental results. Based on the calibrated new dc model, we derive noise models of 18nm DG JL pMOSFETs and show the calculated results using these analytical models for the channel thermal noise, induced gate noise, and their correlation, respectively for the first time.

2. Charged-Based DC Models

Because the DG JL MOSFET(**Fig. 1**) has same type of doping between the source/drain and gate, it is normally on. Therefore, it is important for the JL device to have a small cross section in order to fully deplete the carriers in the channel and turn off the device. This is realized by high doping concentration in the channel: the higher the channel doping concentration is, the smaller the channel cross section will be. However, with such a high doping concentration, it results in degenerate semiconductor and we need to modify the diffusion coefficient D_p by [3]

$$D_p = \frac{kT}{q}\mu_p\left[1+0.35355\left(\frac{n}{N_C}\right)-9.9x10^{-3}\left(\frac{n}{N_C}\right)^2+4.45x10^{-4}\left(\frac{n}{N_C}\right)^3-\cdots\right] \quad (1)$$

In addition, for channel length in the 18 nm range, we need to include the mobility degradation due to the vertical and lateral fields from the gate and drain biases, which is given by

$$\mu_{eff} = \frac{\mu_0}{(1+\theta\cdot V_{GSeff})\sqrt{1+\left(\frac{V_{DSeff}/L}{E_c}\right)^2}} \quad (2)$$

where V_{GSeff} and V_{DSeff} are the effective gate-to-source and drain-to-source voltages, respectively, and the doping dependent critical field E_C is 800 kV/cm. With the modified diffusion coefficient in (1) and the mobility degradation in (2), we calculate the drain current I_{DS} by [2]

$$I = \frac{W}{L}\cdot D_{dg}\cdot\left(\int_S^D \mu_{eff}(V)\cdot q\cdot N_A\cdot T_{SC}\cdot dV - \int_S^D \mu_{eff}(V)\cdot Q_{SC}\cdot dV\right) \quad (3)$$

where $q = 1.6\times10^{-19}$ C, N_A is the density of the acceptor, T_{SC} is the channel thickness, D_{dg} is the term (1 + 0.35355·(n/N_c) - …) in (1), and Q_{SC} is the charge density in the channel [2]. As shown in **Fig. 2**, our new model gives a much better agreement with the measured results.

3. Noise Models

3.1 Channel Thermal Noise Modeling

For the noise calculation at the drain terminal, we used the dc model in (3). Based on the approach described in [4], the power spectral density (PSD) of the total channel thermal noise at the drain terminal will be

$$S_{i_d^2} = \int_0^L \left|\Delta A_d\right|^2 \cdot S_{\delta i_n^2} dx \quad (4)$$

where $S_{\delta i_n^2}$ is the PSD of the local noise current at the position x in the channel, and ΔA_d is the transfer function that convers the local noise current generated at the position x to the drain terminal. From (4), the total channel thermal noise at the drain terminal is given by

$$S_{i_d^2} = 4\cdot k\cdot T_L\cdot\frac{W}{L}\cdot\frac{\mu_0^2\cdot D_{dg}}{\mu_{eff}(V)}\cdot\left(q\cdot N_A\cdot T_{SC}-Q_{SC\_tot}\right) \quad (5)$$

where

$$Q_{SC\_tot} = \int_0^L Q_{SC}(x)dx \quad (6)$$

As we can see in **Fig. 3** and **Fig. 4**, the channel thermal noise is smallest at V_{DS} = 0 V because Q_{SC}, the total channel mobile charge that moves away from the channel to the source and drain terminals, is the highest. When a lot of Q_{SC} is moved away from the channel, the channel is almost

fully depleted, and the device is turned off: Q_{SC} is about same as $q \cdot N_D \cdot T_{SC}$. Under this condition, the thermal noise becomes extremely small, because there are not many mobile carriers in the channel to produce the thermal noise.

3.2 Induced Gate Noise Modeling

Following the same approach as we did for the channel thermal noise, the PSD of the induced gate noise at the gate terminal is given by

$$S_{i_g^2} = \frac{k \cdot T_L \cdot \omega^2 \cdot W \cdot L^3 \cdot \mu_0^2 \cdot {C_{SC}}^2}{\mu_{eff}^3(V) \cdot D_{dg} \cdot \left(q \cdot N_A \cdot T_{SC} - Q_{SC\_tot}\right)} \quad (7)$$

where C_{SC} is the channel capacitance,

$$C_{SC} = \frac{1}{2} \cdot \frac{dQ_{SC}}{dV_{GS}} \quad (8)$$

When the gate bias increases, the PSD of the induced gate noise at 1 GHz is almost constant (**Fig. 5**), which is similar to the experimental results for the conventional MOSFET [5]. Again, when channel is fully depleted, the calculated result is extremely small because the device is about off.

3.3 Correlation Noise Modeling

Finally, the PSD of the correlation noise can be calculated by

$$S_{i_d i_g^*} = -j2 \cdot k \cdot T_L \cdot \omega \cdot L \cdot \left(\frac{\mu_0}{\mu_{eff}}\right)^2 \cdot C_{SC} \quad (9)$$

Fig. 6 shows the magnitude of the PSD of the correlation noise at 1 GHz versus gate voltage characteristics. We noticed that the correlation noise does not have a strong gate bias dependence as that shown in the conventional MOSFETs [5]. This is due to the fact that ΔA_g of the induced gate noise is dominant when compared with ΔA_d of the channel thermal noise in 18nm DG JL pMOSFETs.

4. Conclusions

We demonstrated that doping dependent diffusivity, field dependent mobility, and doping dependent critical electric field are three important effects to be included in the dc model of deca-nm DG JL pMOSFETs and verified it using the experimental results. Based on the physical noise models derived in this paper, we observed that the correlation noise in the 18nm DG JL pMOSFETs does not have a strong gate bias dependence, compared to that in the conventional MOSFETs.

References

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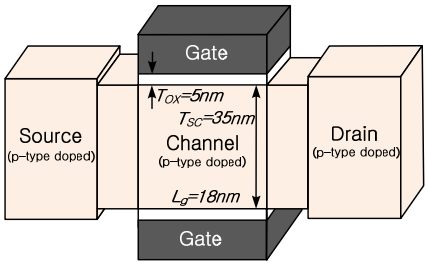

Fig. 1 Physical structure of a double-gate, junctionless doped pMOSFET

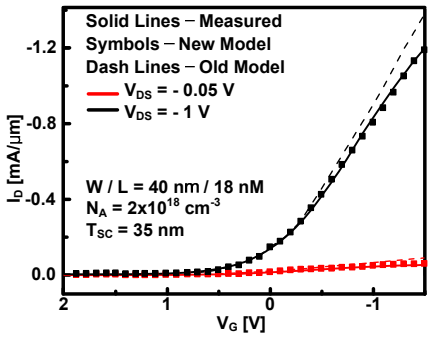

Fig. 2 Drain current versus gate voltage characteristics for 18nm DG JL pMOSFET using the measured results (Solid lines), old model with a constant μ (Dash lines) and our proposed dc model with μ_{eff} for degenerate semiconductor (symbols)

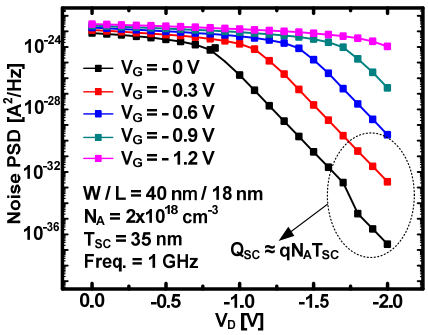

Fig. 3 Calculated PSD of the channel thermal noise versus drain voltage characteristics for a DG JL pMOSFET biased at V_{GS} = -0 V, -0.3 V, -0.6 V, -0.9 V, and -1.2 V, respectively

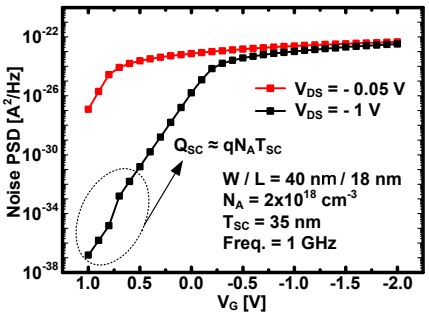

Fig. 4 Calculated PSD of the channel thermal noise versus gate voltage characteristics

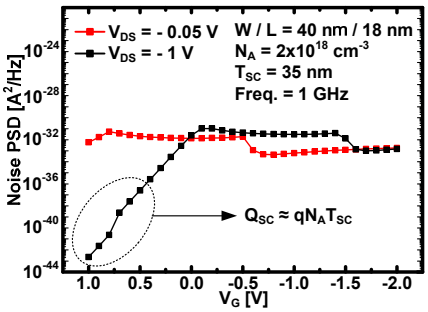

Fig. 5 Calculated PSD of the induced gate noise at 1 GHz versus gate voltage characteristics

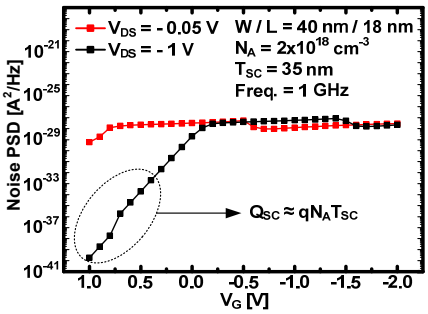

Fig. 6 Calculated magnitude of the PSD of the correlation noise at 1 GHz versus gate voltage characteristics