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Strain Effects on Monolayer MoS_2 Field Effect Transistors

Lang Zeng[1,*], Zheng Xin[1,2], Pengying Chang[1,2] and Xiaoyan Liu[1,*]
[1] Key Laboratory of Microelectronic Devices and Circuits (MOE), Institute of Microelectronics, Peking University, Beijing, 100871, China
[2] School of Electronic and Computer Engineering, Peking University, Shenzhen, 518055, China
Email: Langzeng@ime.pku.edu.cn, xyliu@ime.pku.edu.cn

Abstract

In this work, the strain effect on monolayer MoS_2 field effect transistors is investigated with DFT calculation and quantum transport simulation. DFT calculation reveals that the tensile strain decreases effective mass while compressive strain increases effective mass. However, quantum transport simulation shows smaller effective mass does not always respond to better performance. This is because for FETs at ultimate scaling region, suppression of off-state tunneling current is the biggest concern for device design.

1. Introduction

The continuous scaling of field effect transistors (FETs) in transport direction also demands corresponding scaling in device vertical direction for enough gate controllability [1]. This fact explains why nowadays two dimensional (2D) materials have obtained so much attention [2]. 2D materials can provide atomic layer thickness as well as the elimination of body thickness fluctuation [3].

Among 2D materials, monolayer MoS_2 stands out due to its large intrinsic energy gap and moderate mobility. There exists much theoretical and experimental work on monolayer MoS_2 FETs [3-5]. However, a comprehensive investigation on strain effect on MoS_2 FETs at ultimate scaling region to elucidate device design concerns is still highly demanded.

In this work, we present a DFT calculation and quantum transport simulation combined work that reveals strain effects on effective mass and device performance at scaling limit.

2. Simulation Methods

The atomic structure of monolayer MoS_2 is shown in Fig. 1. Density functional theory (DFT) approach with ultra-soft pseudo-potential (USPP) implemented in CASTEP package is employed to perform the calculation [6]. Exchange and correlation energy is approximated by generalized gradient approximation (GGA) with PW91 [7]. The energy cutoff for charge density is set to be 600 eV. Periodic boundary condition is used to relax all the structures. Biaxial strain is considered in the calculation. Geometric optimization is completed until the maximum force is less than 0.02 eV/Å.

Non-equilibrium Green's function method with effective mass Hamiltonian is employed for the quantum transport simulation. Double gate FET structure is used and is shown is Fig. 1. The Equilibrium Oxide Thickness (EOT) of gate dielectric is 1 nm, and the gate length is chosen to be 10 and 5 nm. The source (drain) is heavily doped with a doping concentration of 8.5×10^{17} m^{-2}, and its length is L_S (L_D) = 10 nm in simulation. The channel is intrinsic, and its length is equal to the gate length. The thickness of monolayer MoS_2 is 0.8 nm and electron density is assumed distributed averagely along vertical direction. Poisson equation is solved self-consistently with the Schrödinger equation over the transport direction.

3. Results and Discussions

The electronic structure of monolayer MoS_2 with different strain conditions by DFT calculation is shown in Fig. 2. It can be seen that tensile strain (up to 3%) can push down the conduction band minima while keep it at K point. The 1% compressive strain can push up the conduction band minima as well as 3% compressive strain shift it away from K point. The extracted band gap and effective mass along KM and ΓK direction is shown in Table. I. Tensile strain decreases both band gap and effective mass, and compressive strain increases them. It is worth noting that our calculation results agree well with self-consistent GW_0 ($scGW_0$) calculation [8].

The simulated output and transfer characteristic curve for monolayer MoS_2 FETs with L_g of 10 nm and 5 nm is shown in Fig. 3 and 4. The off-current of 100 nA/μm is achieved by tuning gate workfunction. It should be noted that: (i) For suppression of strong tunneling effect for L_g = 5 nm, a low workfunction metal should be chosen thus lead to small on-current. (ii) For L_g = 10 nm, the tensile strain with smaller effective mass lead to higher on-current. While for For L_g = 5 nm, the compressive strain with larger effective mass lead to higher on-current. The off-state current density spectrum is shown in Fig. 5 and 6. Although the off-current is pinned to 100 nA/μm, their distributions for L_g = 10 and 5 nm is quite different.

The sub-threshold slope (SS) and drain induced barrier lowering (DIBL) for L_g = 10 and 5 nm with different strain conditions is shown in Fig. 7 and 8. It is observed that SS and DIBL for L_g = 10 nm is almost independent of strain conditions while they have strong dependence on strain conditions for L_g = 5 nm.

The gate capacitance C_g and intrinsic delay for L_g = 10 and 5 nm with different strain conditions is shown in Fig. 9 and 10. It is surprisingly that the intrinsic delay for L_g = 5nm is larger than that of 10 nm, which contradicts with ref. [9]. The reason is two folded: (i) Our gate dielectric EOT is 1 nm while that in ref. [9] is 0.47 nm. The relatively large EOT cannot exploit the advantage of 5 nm short channel length. (ii) The effective mass in our simulation is much smaller than that of ref. [9] (0.579 m_0). This indicates for ultimate short channel devices, a careful device design should be taken for suppresion of tunneling off-current and better performance.

4. Conclusions

This work reveals that compressive strain increases the effective mass of monolayer MoS_2 and tensile strain decreases effective mass. For L_g = 10 nm devices, smaller effective mass correspond to better performance. However, for L_g = 5 nm, a careful and optimized device design should be made to take advantage of smaller effective mass.

Acknowledgements

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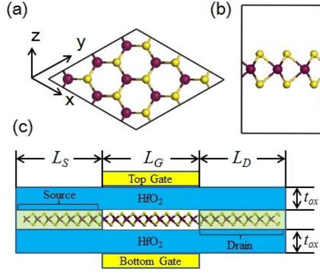

Fig. 1 Sketch of atomic structure of monolayer MoS_2 (a) and (b). Also shown is a diagram of monolayer MoS_2 double gate FETs.

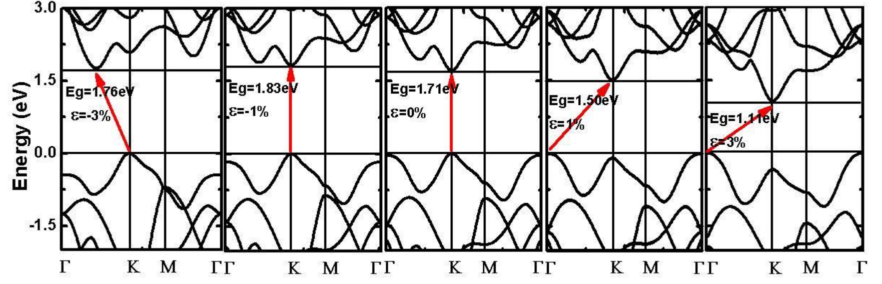

Fig. 2 The electronic structure of monolayer MoS_2 with different strain conditions. The tensile strain (up to 3%) can push down the conduction band minima while keep it at K point. The 1% compressive strain can push up the conduction band minima as well as 3% compressive strain shift it away from K point.

Strain	-3%	-1%	0%	1%	3%
a (Å)	3.07	3.13	3.16	3.20	3.26
Eg (eV)	1.76	1.83	1.71	1.50	1.07
m_e (m_0) KM	0.4226	0.3778	0.3498	0.3290	0.3021
m_e (m_0) ΓK	0.4305	0.3716	0.3435	0.3211	0.2945

Table. I Lattice constant, energy gap, effective mass along KM and ΓK directions for different strain conditions.

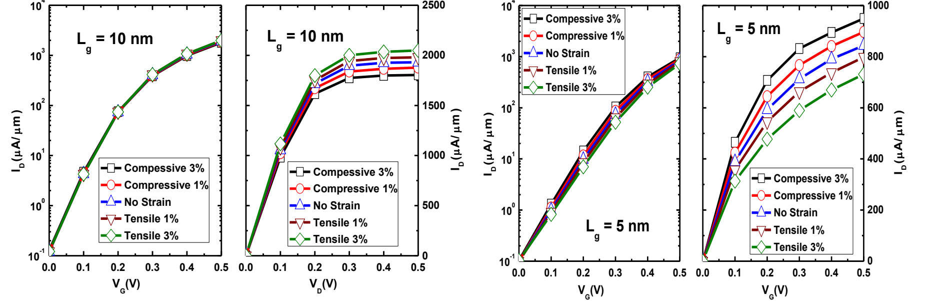

Fig. 3 The transfer (left) and output (right) characteristic curves for L_g = 10 nm. It can be seen that 3% tensile strain has best performance.

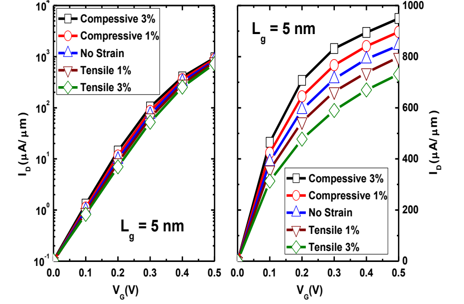

Fig. 4 The transfer (left) and output (right) characteristic curves for L_g = 5 nm. It can be seen that -3% compressive strain has best performance.

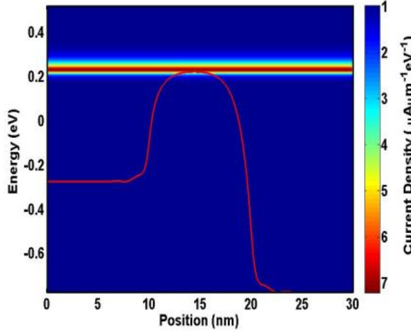

Fig. 5 Current density spectrum for off-state (V_g = 0 V and V_d = 0.5 V) with L_g = 10 nm.

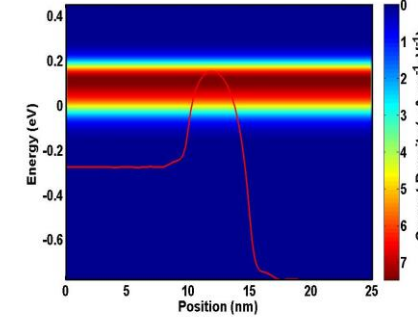

Fig. 6 Current density spectrum for off-state (V_g = 0 V and V_d = 0.5 V) with L_g = 5 nm.

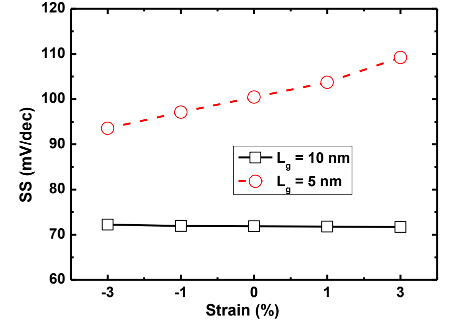

Fig. 7 Sub-threshold slope for L_g = 10 and 5 nm with different strain conditions.

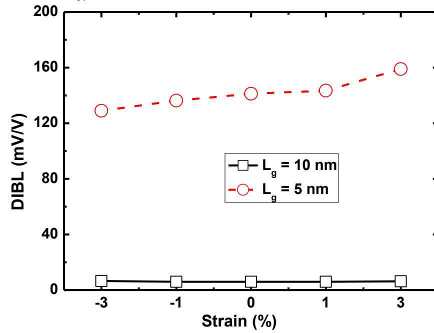

Fig. 8 Drain induced barrier lowering for L_g = 10 and 5 nm with different strain conditions.

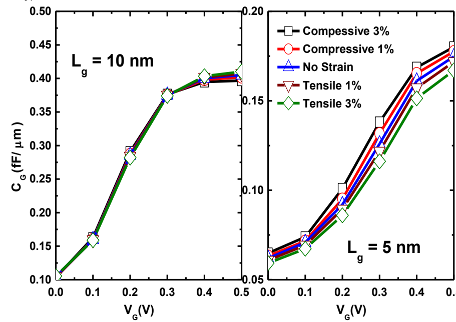

Fig. 9 Gate capacitance C_g for L_g = 10 (left) and 5 nm (right) with different strain conditions.

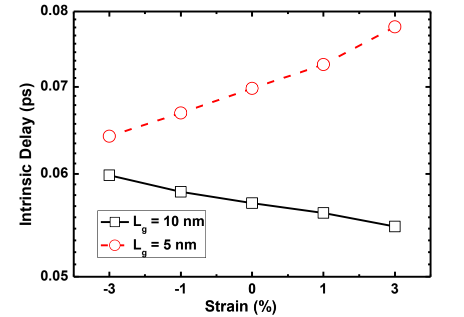

Fig. 10 Intrinsic delay for L_g = 10 and 5 nm with different strain conditions.