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Impact of Trap Behavior in High-k/Metal Gate p-MOSFET with Incorporated Fluorine on Low-Frequency Noise Characteristics

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Abstract

Impact of Fluorine (F) implantation on 1/*f* noise and random telegraph noise (RTN) characteristics in High-k/Metal Gate (HK/MG) pMOSFETs are investigated. In addition, incorporation of F has been identified as an effective method for passivating oxygen vacancies and defect sites and controlling V_T in PMOS. Then RTN and 1/*f* results found that irrespective of the implanted dose, HK/MG devices with F implanted exhibited lower slow oxide trap densities to the control device.

1. Introduction

Low-Frequency (LF) noise is a useful characterization technique for the study of slow oxide or border traps in the gate dielectric of a MOSFET. For sub-28-nm era, issues of direct gate tunneling, poly-gate depletion, gate sheet resistance, boron penetration, and Fermi level pinning [1] become the severe obstructions for performance improvements. To eliminate these problems, high-permittivity (HK) materials and metal gate (MG) electrodes have extensively replaced conventional SiO_2 gate oxide and poly-gate, respectively. However, fabricating a metal gate p-type metal–oxide–semiconductor (PMOS) transistor with low threshold voltage (V_T), especially with a small equivalent oxide thickness (EOT), is crucial in gate-first integration owing to the presence of various oxygen vacancies and defect sites in the HK gate dielectric. Recently, incorporation of F has been identified as an effective method for passivating oxygen vacancies and defect sites [2] and controlling V_T in PMOS [3]. However, to obtain large V_{FB} shift with minimized EOT penalty in HK/MG pMOSFETs, aluminum (Al) ion implantation (I/I) technology was implemented and identified as an effective approach for effective work function (EWF) modulation without EOT increasing and complicated process [4]. On the other hand, the low frequency noises including 1/*f* noise and RTN in device drain currents (I_D) has been used for many decades as an indicator of device performance and reliability, which is attributed to the random trapping/detrapping process of signal or multiple traps in the gate dielectric, results in two discrete current levels in the time domains. By characterizing of RTN as a function of temperature or bias dependence, the energy level, capture and emission kinetics, and spatial location of traps can be obtained. Especially, the analysis on RTN in HK/MG stacks devices to determine whether an oxide trap leading to RTN is located in high-k layer or in interfacial layer (IL) and then to characterize such a trap will be beneficial to develop new process flow evolution. In this paper, we present the correlation between RTN and 1/*f* noise parameters in HK/MG stacks pMOSFETs with F into the HK gate dielectric and Al I/I.

2. Device Structure and Experiment

For the experimental work, all pMOSFETs devices were fabricated using 28 nm gate-first (HK/MG) technology. The gate dielectrics consist of a 1 nm thermal-grown SiO_2 as an IL, followed by a 2.5 nm atomic layer deposition on HfO_2 HK film. In F channel implantation experiments, 2×10^{15} cm^{-2} (device A) and 5×10^{15} cm^{-2} (device B) doses of F were implanted at 10 keV through a 4-nm-thick layer of sacrificial oxide, and then oxide mask was removed and subsequently fresh core oxide was grown. A rapid thermal spike (RTP) annealing was performed at 930˚C to manipulate the F distribution profile after implantation. A 10 nm radio-frequency PVD TiN was deposited as gate metal, Al ion implantation through TiN layer was performed at 1.2 keV with dose of 5×10^{15} cm^{-2}. For comparison, HK/MG pMOSFETs without F implanted were also fabricated and labeled as control device.

3. Results and Discussion

Fig. 1 shows the drain current (I_D) as a function of drain voltage (V_D) for all HK/MG pMOSFETs. Approximately 4 and 11% I_D enhancement obtained for device A and B, respectively, as compared with the control device at a fixed gate overdrive, V_G - V_T = -0.8 V, and V_D = -1.0 V. The V_T for device A, B, and the control are -0.51 V, -0.48 V, and -0.55 V, respectively in Fig. 2. The results indicated that F implanted, make a decline in the number of interface traps. F is thought to segregate at the HfO_2/SiO_2 and SiO_2/Si interfaces and effectively to passivate interface charge-trapping sites, consistent with the higher PMOS V_{FB} that is associated with a lower interface state density and fewer oxygen vacancies [5]. To investigate the impact of F implanted on 1/*f* noise of HK/MG devices, the normalized drain current noise spectral density S_{ID} for all HK devices taken from the average of six devices biased at different gate overdrive voltages are presented as Fig. 3. All devices show typical 1/*f* noise type with the frequency exponent close to unity for all gate overdrives. The noise level in devices A and B is observed to be significantly lower than the control with no F implanted, which implies high-k layer has lower trap density. The normalized drain current noise spectral density (LS_{ID}/I_D^2) and the transconductance to drain current squared $(g_m/I_D)^2$ as function of drain current are plotted in Fig. 4 to confirm the physical mechanism of 1/*f* noise. The LS_{ID}/I_D^2 was extracted at f = 25 Hz for all devices. The LS_{ID}/I_D^2 curve of all devices shows cannot follow this trend at high current with $(g_m/I_D)^2$, which imply that either of the correlated mobility fluctuation ($\Delta\mu$) or source/drain (S/D) series resistance is major noise mechanism and need to be clearly clarified [6]. Using Fig. 5, all devices shows $(V_G - V_T)^{-m}$ with m ~ 0.97 for all devices, which highlights that the noise contribution of the series resistance to the overall noise is negligible. In order to further evaluate the parameters of 1/*f* noise model on all devices, the normalized input-referred voltage noise spectral density (LS_{VG}) as a function of the V_G - V_T is shown in Fig. 6. As expected, all devices show two distinct regions in the associated LS_{VG}. In region I ($|V_G - V_T| \le 0.2V$), the LS_{VG} is independent of V_G - V_T, which indicate a signature of number fluctuations. In region II ($|V_G - V_T| > 0.2V$), a pronounced LS_{VG} dependence on V_G - V_T indeed proves that correlated mobility fluctuations were involved.

In the all devices, LS_{VG} shows a tendency to flatten out from low $V_G - V_T$ to high $V_G - V_T$ indicating a number fluctuation origin. The number fluctuation model, including correlated mobility fluctuation, takes the following form

$$LS_{VG} = \frac{q^2 KT}{WC_{ox}^2 f^r} \lambda N_t \left[1 + \alpha \mu_0 C_{ox} (V_G - V_T)\right]^2 \qquad (1)$$

where λ is the tunneling attenuation length for channel carriers penetrating into the gate dielectric, Nt is the effective near interface oxide trap density, α is a scattering coefficient, and μ_0 is the low field mobility. The LS_{VG} level in region I was correlated with λNt, as shown in the first term in the parentheses in (1). The second term in the parentheses presents correlated mobility fluctuations, which can be dominated in region II. The extracted mean capture time (τ_c) and mean emission time constant (τ_e) versus gate overdrive (V_G - V_T) are presented in Fig. 7. It can be found that the devices A and B with F implanted shows the lower values of τ_c and τ_e and the weak dependence of τ_e on $V_G - V_T$, indicating that the position of trap is closer to the IL/Si interface. Fig. 8 shows the dependence of the $\ln(\tau_c / \tau_e)$ with respect to the V_G - V_T for all devices. The dashed lines represent linear fitting curve to extract the trap depth (x_t), away from the SiO_2 IL/Si interface, using the conventional method [7]. Interestingly, the trap position x_t will shift from 2.1 nm in the HK dielectric for the control to 1.82 nm (1.68 nm) for device A (B) with F implanted. Although the trap for all devices is located in the high-k material layer, device B is closer to the SiO_2 IL/Si interface. The smaller x_t implies the reduction λ, which is an important parameter in 1/*f* noise. The relation between x_t and λ can be express as

$$Xt = \lambda \cdot \ln(1/2\pi f \tau_0) \qquad (2)$$

where the time constant τ_0 is often taken as 6.6×10^{-14} s [8]. The λ values for hole tunneling at a *f* = 25 Hz were calculated as 8.3×10^{-9}, 7.31×10^{-9}, and 6.72×10^{-9} cm for the control, device A, and B, respectively. Moreover, calculated from the data in Fig. 6, and slow oxide trap densities shown in Fig. 9, we found that the extracted N_t were 5.28×10^{18}, 3.49×10^{18} and 9.62×10^{17} cm^{-3} ev^{-1} for the control, device A and B, respectively. As clearly reported in review paper [9] Al I/I in HK/MG devices has little influence on trap density, so we increased the F implanted, effective method for passivating oxygen vacancies and defect sites. However, the implantation energy and dose to obtain F distribution profile shifted toward HfO_2/SiO_2 and SiO_2/Si interface without degradation in reliability and performance should be well controlled by the optimized process.

4. Conclusions

We have investigated the trap behavior in pMOSFETs with different concentrations of F into the HK gate dielectrics by using 1/*f* noise and RTN measurements simultaneously. Compared with the control device, device A and B with considerably lower 1/*f* noise level was observed, which is resulting from the decrease in λ. The x_t of devices B closer to SiO_2 IL/Si interface maybe resulted from for F passivating oxygen vacancies and defect sites.

Acknowledgements

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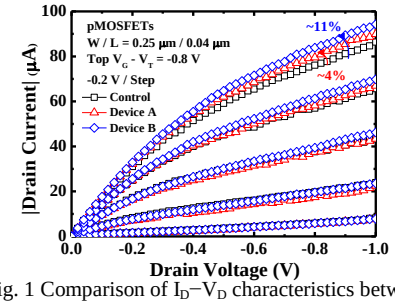

Fig. 1 Comparison of I_D–V_D characteristics between the HK/MG pMOSFETs with F implanted and the control device.

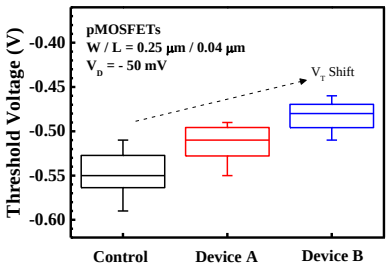

Fig. 2 Threshold voltage characteristics of pMOSFETs with F implanted and the control device.

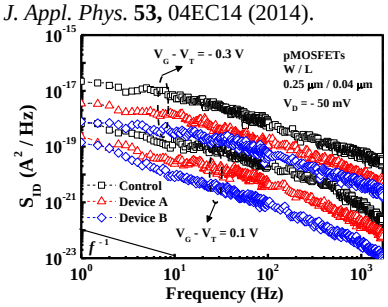

Fig. 3 The normalized drain current noise spectral density S_{ID} for all HK/MG pMOSFETs.

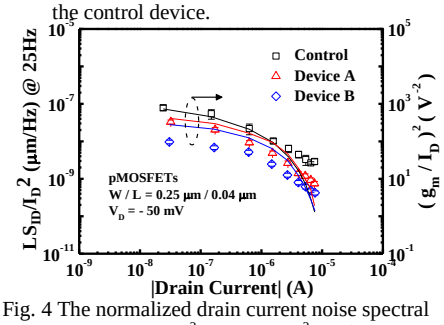

Fig. 4 The normalized drain current noise spectral density LS_{ID}/I_D^2 and $(g_m/I_D)^2$ as function of drain current for all HK/MG pMOSFETs.

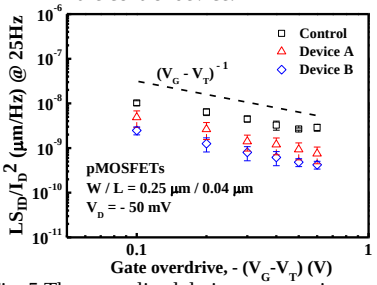

Fig. 5 The normalized drain current noise spectral density S_{ID}/I_D^2 at *f* = 25 Hz as function of gate overdrive (V_G-V_T).

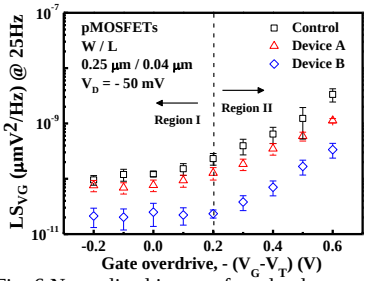

Fig. 6 Normalized input-referred voltage noise spectral density LS_{VG} versus gate overdrive for all HK/MG pMOSFETs.

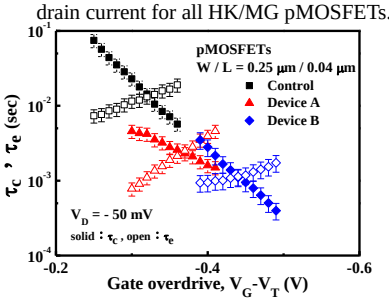

Fig.7 Comparison of the capture time (solid) and emission time (open) for all devices.

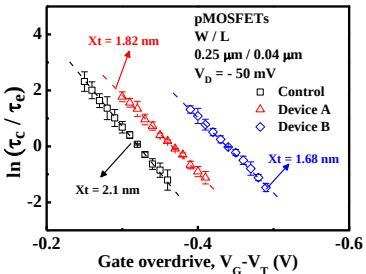

Fig.8 Plot of capture time (τ_c) over emission time (τ_e) versus gate overdrive for the HK/MG pMOSFETs.

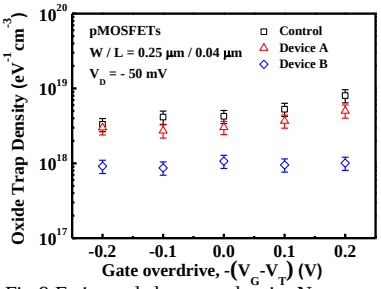

Fig.9 Estimated slow trap density Nt versus gate overdrive at V_D = -50 mV for all HK/MG pMOSFETs.