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Electrical Characteristics of Novel Junctionless FinFET Utilizing Trench Structure for Extreme Scaling

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I. Abstract

This work describes the fabrication of a trench junctionless field-effect transistor (JL-FET) with ultra-thin channel thickness, by using the dry etching process. Experimental results confirm the excellent performance of the trench JL-FET with nanowires (NWs) at a subthreshold swing (SS) of 109 mV/dec., an I_{ON}/I_{OFF} ratio of 10^7 A/A, and a low drain-induced barrier lowering (DIBL) value of 5 mV/V. Moreover, the trench JL-FET can further increase the device I_{ON}/I_{OFF} ratio, and SS. Importantly, owing to its excellent device characteristics and simple fabrication, the trench JL-FET is highly promising for use in advanced three-dimensional (3-D) stacked ICs applications.

II. Introduction

While fabricated using the dry etching process, the trench JL-FET is used to form a trench and define channel thickness (T_{CH}) and gate length (L_G). Recently, investigations have distinguished the JL-FET from a conventional inversion mode (IM) MOSFET in terms of structure and operating principles. The JL-FET is fabricated simply by heavily doping the channel and source/drain (S/D) regions simultaneously [1]-[5]. Moreover, the short channel effect (SCE) can be minimized while achieving a high drive current at an extremely-scaled down L_G of the JL-FET [6]. In this work, we further study the effects of different structural parameters, including the T_{CH} and L_G, on the characteristics of the trench JL-FET device. The trench JL-FET with nanowires (NWs) performs better than the JL-FET without trench, owing to its thin channel structures [7]-[8].

III. Experiment

The trench JL-FET was fabricated by first growing a 400 nm thermal silicon dioxide layer on 6 inch silicon wafers as substrates. A 50 nm undoped amorphous silicon (a-Si) layer was then deposited by low-pressure chemical vapor deposition (LPCVD) at 550 ^oC. Next, the a-Si layer was solid-phase recrystallized (SPC), subsequently forming a large grain size at 600 ^oC for 24 hrs in a nitrogen ambient atmosphere. The SPC layer was implanted by 16-keV with phosphorous ions at a dose of 2×10^{14} cm^{-2}, followed by furnace annealing at 600 ^oC for 4 hrs. The device's active NWs were patterned by electron beam (e-beam) direct writing and transferred by reactive-ion etching (RIE). The trench structure with 15-nm-thick channels was subsequently defined by e-beam lithography and isotropic etched by time-controlled RIE. Next, a 10 nm dry-oxide, consuming 10 nm poly-Si to form 5 nm channels, was deposited as the gate oxide layer. Simultaneously, the L_G was defined by the trench structure. Additionally, 150 nm in-situ doped n^+ poly-silicon deposition was performed as a gate electrode and patterned by e-beam lithography and RIE. Moreover, a 200 nm SiO_2 passivation layer was deposited. Finally, 300 nm Al-Si-Cu metallization was performed and sintered.

IV. Results and Discussion

Fig. 1 schematically depicts the JL-FET with and without trench structure that provides detailed information of the process flowchart. Fig. 2(a), (b) presents the atomic force microscopy (AFM) images of the channel region of the trench JL-FET, and fig. 2(c), (d) displays the top view scanning electron microscope (SEM) image of that with L_G = 0.5 μm.

Fig. 3(a) presents the transmission electron microscopic (TEM) images of the L_G is 0.27 μm and the T_{CH} is 4.18 nm. Fig. 3(b) presents the TEM images of the L_G is 0.5 μm and the T_{CH} is 2.8 nm with an effective width of 68 nm×10.

Fig. 4 shows the I_D-V_G characteristics of the trench JL-FET (T_{CH} = 2.8nm) and the JL-FET without trench (T_{CH} = 25 nm) with L_G = 0.2 μm and 0.5 μm. The trench JL-FET device has a steeper SS (117 mV/dec.), more appropriate threshold voltage (V_{TH} = -0.19 V) and higher I_{ON}/I_{OFF} ratio (1.41×10^7 A/A).

Fig. 5 plots the I_D-V_G characteristics of the trench JL-FET with different L_G ranging from 0.2 μm to 0.5 μm. The SS values of all devices are approximately 100 mV/dec. Owing to the ultra-thin T_{CH} which can provide good gate controllability and an I_{ON}/I_{OFF} ratio of around 10^7 A/A. The long channel (L_G = 0.5 μm) devices have a thinner T_{CH} under higher etching rate.

Fig. 6 compares the typical characteristics of the trench JL-FET with tri-gate structure (W_{eff} = 68 nm ×10) and planar gate structure (W_{eff} = 1 um). The device with tri-gate has a steeper SS (110 mV/dec.) and a lower DIBL value of 5 mV/V.

Fig. 7 shows the DIBLs of JL-FET with and without trench. The inset of fig. 7 compares the mean values of DIBLs at different L_G ranging from 0.2 μm to 1 μm for the JL-FET with and without trench. The trench JL-FET devices have a superior DIBL which is approximately 0 mV/V.

Fig. 8 compares the I_D-V_D output characteristics of the JL-FET with and without trench for the same L_G = 0.5 μm. The trench JL-FET has a higher saturation current this result could be owing to quantum confinement effect.

Table I. compares the JL-FET with important parameters. The great SS and V_{TH} depend on the multi-gate structure and T_{CH}.

V. Conclusion

This work described the fabrication of a novel trench JL-FET, along with its characteristics. Experimental results indicate that the trench structure was successfully and easily integrated into the JL-FET device, subsequently improving the device performance. Fabricating the trench structure is simple and compatible with dry etching process of current CMOS technologies. Additionally, the trench JL-FET with NWs has excellent electrical characteristics. The trench JL-FET is highly promising for use in 3-D stacked ICs applications.

VI. References

[1] J. P. Colinge et al., APL, 2010, vol. 96, no. 7, pp. 073510 - 073510-3.

[2] H. C. Lin et al., EDL, 2012, vol. 33, no. 1, pp. 53 - 55.

[3] R. Rios et al., EDL, 2011, vol. 32, no. 9, pp. 1170 - 1172.

[4] C. W. Lee et al., APL, 2010, vol. 96, no. 7, pp. 073510 – 073510 -3.

[5] S. J. Choi et al., EDL, 2011, vol. 32, no. 2, pp. 125 - 127.

[6] C. W. Lee et al., SSDM, 2010, pp.1044 -1045.

[7] H. B. Chen et al., VLSI, 2013, pp. 232 - 233.

[8] S. Migita et al., IEDM, 2012, pp. 194.

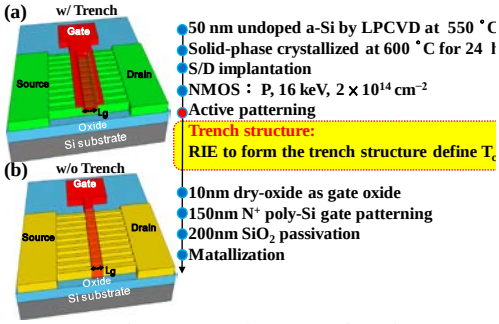

Fig. 1 The details of the process flowchart of the fabricated d
vided as well. Fig. 1(a)-(b) Schematic diagram of the JL-FET
out trench device.

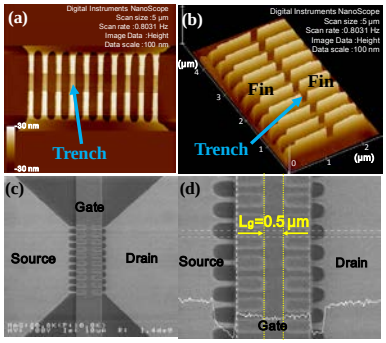

Fig. 2(a)-(b) The AFM images of the channel region of the t
Fig. 2(c)-(d) The top view SEM images of the trench JL-FET
μm.

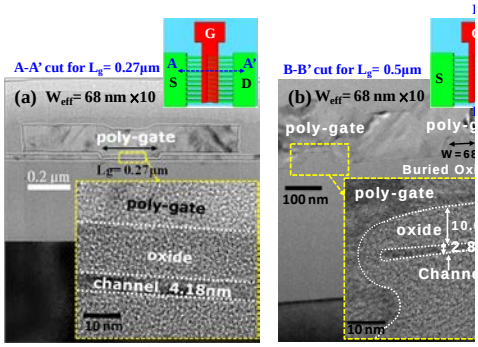

Fig. 3(a) TEM images of trench JL-FET with L_G = 0.27 μm a
nm. (d) TEM images of trench JL-FET with L_G = 0.5 μm and
The effective channel width is 68 nm × 10.

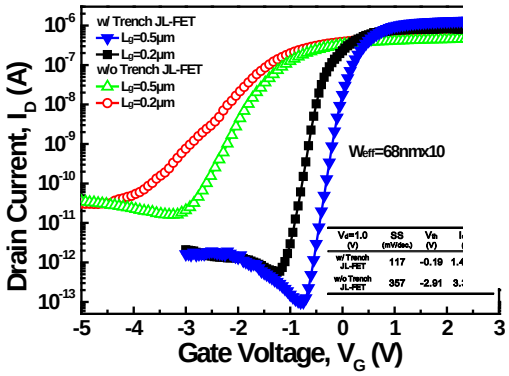

Fig. 4 Comparison of the I_D-V_G curves of the JL-FET with and without trench
at L_G = 0.2 μm and 0.5 μm.

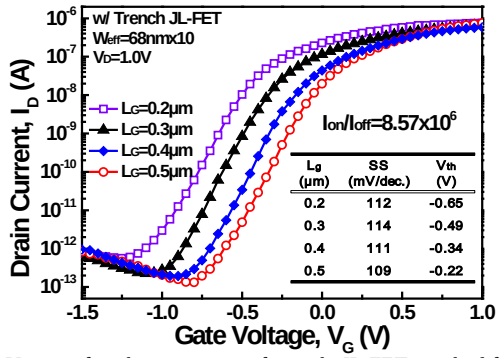

Fig. 5 I_D-V_G transfer characteristics of trench JL-FETs with different L_G,
ranging from 0.2 μm to 0.5 μm.

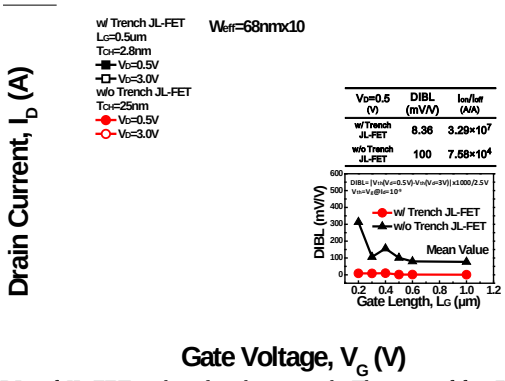

Fig. 7 DIBLs of JL-FET with and without trench. The inset of fig. 7 compares
the mean values of DIBLs at different L_G ranging from 0.2 μm to 1 μm for
JL-FET with and without trench.

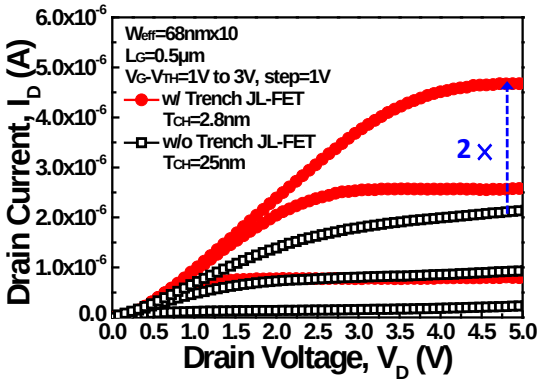

Fig. 8 The I_D-V_D output characteristics of the JL-FET with and without trench
for the same L_G = 0.5 μm.

Table I
Lists important parameters in comparison with the other works

	This work	Ref.[A]	Ref.[B]	Ref.[C]
Channel structure	N-SPC JL-Trigate	N-SPC JL-GAA	N-SPC JL-Planar	N-SPC JL-GAA
W/L (μm/μm)	0.1x10/0.5	0.7x10/1	10/0.4	0.07x2/1
EOT (nm)	10	17	8	15
T_{CH}(nm)	2.38	2	10	12
V_{TH}(V)	-0.22	0.25	-0.15	-0.3
SS(mV/ dec.)	100	61	250	199
I_{on}/I_{off} (V_g:V_d)	>10^6 (2V:1V)	>10^7 (3V:0.5V)	>10^7 (3V:0.1V)	>10^6 (5V:1V)

Ref. [A] H. B. Chen et al., VLSI, pp. T232, 2013. Ref. [B] H. C. Lin et al.,
TED, pp. 1142, 2013. Ref. [C] C. J. Su et al., EDL, pp. 521, 2011.