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Multilevel Storage and its Cycling in $Ge_1Sb_4Te_7$ Phase-Change Memory

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Abstract

In this work, $Ge_1Sb_4Te_7$ (GST) was adopted as the storage media for multiple resistance levels. It was exhibited that the resistivity of GST gradually dropped for about 3-4 orders of magnitude with the annealing temperature, which is critical to realize multi resistance levels. The ultra-multi 23 resistance levels in GST lateral phase-change memory device were demonstrated by controlling the maximum sweeping currents. The cycling of the 6 multi resistance levels, distinguishable from each other, were also demonstrated. This study indicated that GST is a media suitable for stable ultra-multilevel storage, enabling low-cost ultra-high-density nonvolatile memory.

1. Introduction

There is a growing demand for memory nowadays. One of the most effective approaches to increase the memory capacity is the multiple-level storage (MLS), by which much more information can be stored without increasing memory size. Phase-change memory (PCM) based on amorphous-crystalline transition [1-2] is expected to apply to MLS since a lot of intermediate resistance levels become possible by controlling the total crystallinity between electrodes in principle. But practically, most of today's PCMs with a single phase-change chalcogenide layer and an in-series heater exhibit sharp resistance changes with the programming pulse amplitude [3-4], which makes them very difficult to apply to MLS in a stable and controllable way. In order to obtain gradual (or step-like) resistance change characteristics, PCMs with stacked chalcogenide layers were proposed and they exhibited MLS potential. However, the number of storage levels depends strongly on the number of chalcogenide layers and only four-level-storage was demonstrated up to now due to the difficulty in design [5-6]. In this study, we demonstrate the possibility of ultramultiple-level storage (UMLS) by using a lateral Ge1Sb4Te7 (GST)-based structure. The number of distinct resistance levels can readily reach 20 and even higher, depending on programming currents. The cycling of six-level storage was also demonstrated without any help of algorism for programming.

2. Experimental methods

200-nm-thick GST film samples with a $ZnS\text{-}SiO_2$ capping layer on glass substrates were prepared by introducing Ar into the chamber using a radio frequency sputtering equipment (MNS-3000-RF, ULVAC, Inc.) at a background pressure below 5×10^{-5} Pa and a sputtering pressure of 0.2 Pa. Resistivity as a function of annealing temperature of films was measured by using square-shaped film samples ($12\times12\ mm^2$) defined by $TiSi_3$ electrodes. The sample was annealed on a hot plate at each increasing temperature for 3 min. Crystal structures of films were characterized by X-ray diffractometer (RINT 2000, Rigaku co.) after annealed on a hot plate for 3 min. Current-voltage (*I-V*) characteristics of the device samples were measured by semiconductor parameter analyzer (4155B, Agilent Technologies, Ltd.).

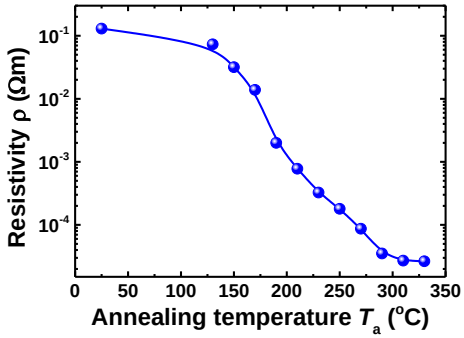

Fig. 1 Resistivity change of $Ge_1Sb_4Te_7$ film when it was annealed at increasing temperatures up to 330°C.

3. Experimental results

Figure 1 shows the relationship between resistivity of GST and annealing temperature up to 330°C in which thickness reduction due to phase change was neglected.

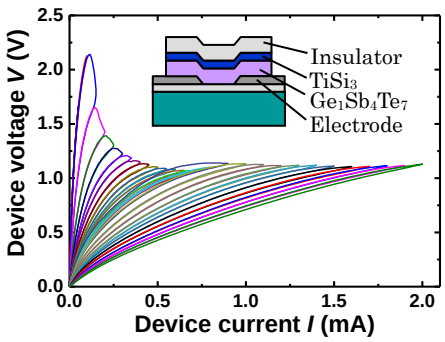

Fig. 2 UMLS in the $Ge_1Sb_4Te_7$ device. *I-V* curves were obtained when currents were swept from 0 mA to the programming current Ip forward and backward. I_p increased from 0.1 to 2 mA.

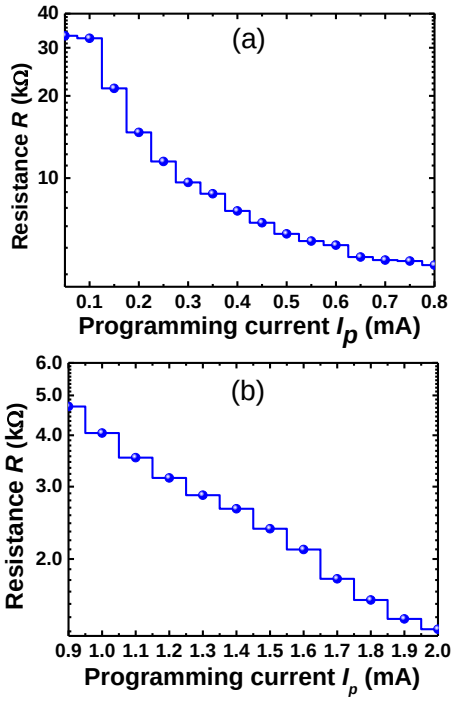

Fig. 3 (a) 13 resistance levels were obtained by programming the device up to 0.8 mA. (b) 12 resistance levels were further obtained by programming the device from 0.9 mA to 2 mA.

Resistivity of as-deposited GST film was as low as around 0.1 Ω·m, which resulted from the fact that the as-deposited GST film was already crystalline based on X-ray diffaction (XRD) analysis. Resistivity of GST film decreased by about 4 orders of magnitude in the range of 110-310°C. The resistivity reduction was due to the phase transformation from face-centered cubic (FCC) to hexagonal (HEX) structure (XRD patterns are not shown here). This gradual resistivity reduction is very important to obtain intermediate resisitance levels for the UMLS applications.

Figure 2 shows the programming of the device by the current sweepings from 0 to the programming currents I_p forward and backward. The programming currents were from 0 to 2 mA with an increasement of 0.05 or 0.1 mA. The active layers of the PCM device consisted of 150-nm-thick GST layer and a top 50-nm-thick $TiSi_3$ layer, as shown in the inset of figure 2. The GST and $TiSi_3$ layers were both deposited using a radio frequency sputtering equipment (MNS-3000-RF, ULVAC, Inc.) at a sputtering pressure of 0.2 Pa. It is very clear that the intermediate levels were very stable because the changed resistance levels can be retained until the sweeping current became higher than the former programming current.

The programmed resistance could be read out at a certain low current or voltage. Figures 3 show the device resistance as a function of the programming current. The first sudden resistance drop due to threshold switching was caused by the crystallization at the steps in the $Ge_1Sb_4Te_7$ layer. The subsequent gradual resistance drops resulted from crystal transformation from FCC to HEX. 13 distinct resistance levels were observed in the low programming currents up to 0.8 mA. 12 resistance levels were further obtained by

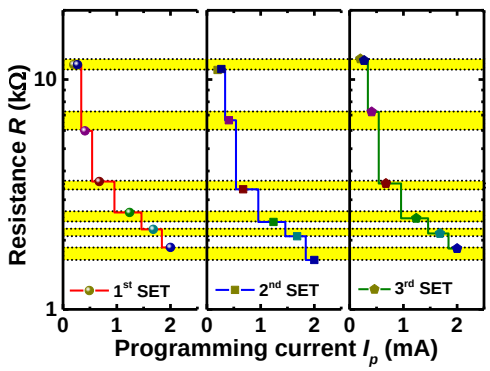

Fig. 4 Cycling demonstration of 6 resistance level storage.

programming the device from 0.9 mA to 2 mA. These resistance levels were well controlled by current-driven Joule heating.

The cycling of 6 resistance level storage was demonstrated in GST device, as shown in figure 4. The device was programing by current sweeping as described above. After each set programming, resistance was reset by voltage pulse applications. It is obvious that these resistance levels are distinct and are able to be repeatedly programmed without any algorism such as write-cerfication [7].

4. Conclusions

A lateral GST phase-change memory with a top heater was proposed and investigated for UMLS. The active layers consisted of a 50-nm-thick $TiSi_3$ layer as a heater and a 150-nm-thick GST layer. Experimental results revealed that a number of intermediate levels were distinct and stable, which were well controlled by the applied currents. The UMLS results from gradual crystal transformation between electrodes by Joule heating. In this work, 25 distinct resistance levels were successfully obtained, which enabled 12.5 times information to be stored in a single device, compared with the conventional binary memory. The cycling of 6-resistance level storage was also demonstrated.

Acknowledgements

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