Rectifying Characteristics of Sol-gel derived TiO\textsubscript{x} thin films for 1D-1R Resistance Switching Memory Applications

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Abstract

We demonstrated a sol-gel processed Ti/TiO\textsubscript{x}/Pt diode for alleviation of the sneak current path in cross point resistive switching memory array. Owing to asymmetric schottky barriers at the Ti/TiO\textsubscript{2} (0.13 eV) and the TiO\textsubscript{x}/Pt (0.57 eV) interface, a high current density (>10\textsuperscript{2} A/cm\textsuperscript{2}) and an on-off ratio (>10\textsuperscript{4}) were achieved. By stacking the Ti/HfO\textsubscript{2}/Pt unipolar resistive memory component on the Ti/TiO\textsubscript{x}/Pt diode for 1D-1R structure, we could significantly reduce the read disturbance from unselected cell.

1. Introduction

Recently, a resistive switching random access memory (ReRAM) based on reversible resistance change in transition metal oxides, such as HfO\textsubscript{2} and ZnO, has been intensively investigated due to excellent scalability, high density, simple structure, low-power consumption. However, a read disturbance owing to crosstalk among neighboring cells is a serious problem for application of high density memory array. Therefore, the unit cell of ReRAM required a selector to prevent undesirable crosstalk. The one diode and one resistor (1D-1R) structures with a high forward current density are used to alleviate the sneak current path and low thermal budget [1].

In this paper, we demonstrated the rectifying characteristics of Ti/TiO\textsubscript{x}/Pt diode fabricated by sol-gel spin coating of TiO\textsubscript{2}. Among the various techniques for oxide thin films deposition, the sol-gel process has attracted a lot of attention because of simplicity, cost effectiveness and minimum plasma damage. The rectifying characteristic of sol-gel based TiO\textsubscript{2} diode with sputter based TiO\textsubscript{2} diode was compared. We demonstrated that the read current in 1D-1R structure consists of sol-gel processed TiO\textsubscript{2} diode and HfO\textsubscript{2} resistive memory was considerably improved.

2. Experimental

As a starting material, the p-type Si (100) wafers with a 300-nm thick thermal oxide are used. The Ti and Pt layers for bottom electrode (BE) are sequentially deposited by 5-nm and 50-nm thick, respectively, using an electron-beam evaporator. And then, the sol-gel solution for TiO\textsubscript{2} thin film is prepared from SYM-TI05 solution (Kojundo Chemical Lab., 0.5 m/L). The TiO\textsubscript{x} solution was diluted with the spin coating of TiO\textsubscript{x}. Among the various techniques for fabricating the Ti/TiO\textsubscript{x} structural diode devices, we could significantly reduce the read disturbance from unselected cell.

Disturbance from unselected cell. The low resistance state (LRS) current (at 1/2V Read, cause the sneak current path) in the unselected cells was due to oxygen deficient state at TiO\textsubscript{2}/Pt interface generates Ti\textsuperscript{3+}, and these Vo act as donor [2]. Therefore, the Fermi level of TiO\textsubscript{2} become closer to the conduction band when the increasing of the V\textsubscript{o}. As a result, SBH at TiO\textsubscript{2}/Pt interface is decreased, so the reverse current in sputtered TiO\textsubscript{2} diode is increase.

Carried out to remove the solvent from the solution-deposited high-k films. The dried substrates were annealed at 600 °C in a conventional furnace in the oxygen ambient for 30 min. The top electrode (TE) with a size of 250 × 160 μm\textsuperscript{2} was formed by Ti deposition and lift-off processes for fabricating the Ti/TiO\textsubscript{x}/Pt structural diode devices. In order to compare with sputtered TiO\textsubscript{2} diode, TiO\textsubscript{2} films were deposited by rf sputtering onto Pt BE at 75 W, Ar 20 sccm, 3 mtorr followed by annealed at 600 °C in the oxygen ambient. For the 1D-1R memory cell structure, the Ti/HfO\textsubscript{2}/Pt unipolar resistive memory component was stacked on the the Ti/TiO\textsubscript{x}/Pt diode and the memory behavior were measured.

3. Results and Discussion

Fig. 1 shows the rectifying characteristics of Ti/TiO\textsubscript{x}/Pt diodes. The asymmetrical current density vs. applied voltage (J-V) was due to the difference schottky barrier height (SBH) at the Ti/TiO\textsubscript{x}(TiO\textsubscript{2}) and TiO\textsubscript{x}(TiO\textsubscript{2})/Pt interfaces. It is worth to note that the sputter based Ti/TiO\textsubscript{x}/Pt diodes showed a lower forward current, higher leakage current and poor ideality factor (η).

Fig. 2 shows the temperature-dependent schottky fitting of both devices in forward (a) and reverse (b) current measured from room temperature to 125 °C. The extracted SBH is estimated Φ\textsubscript{Ti/TiO\textsubscript{x}} = 0.13 eV and Φ\textsubscript{TiO\textsubscript{x}/Pt} = 0.57 eV at each interface in sol-gel Ti/TiO\textsubscript{x}/Pt diode. On the other hand, Φ\textsubscript{Ti/TiO\textsubscript{2}} = 0.16 eV and Φ\textsubscript{TIO\textsubscript{2}/Pt} = 0.46 eV for sputtered Ti/TiO\textsubscript{2}/Pt diode. The difference of SBH is larger in sol-gel diode, as shown in insets. That is the reason why the high on-off ratio was achieved in sol-gel TiO\textsubscript{2} diode (>10\textsuperscript{4} in sol-gel diode, >10\textsuperscript{5} in sputtered diode at ±2 V).

In order to indentify the effect of oxygen vacancy (V\textsubscript{o}), X-ray photoelecetron spectroscopy (XPS) was measured as shown in the Fig. 3(a, b). The core level spectra of O 1s can be deconvoluted into two peaks corresponding to lattice oxygen (O-Ti) and non-lattice oxygen (V\textsubscript{o}). As shown in Fig. 3(a), the concentration of non-lattice oxygen at TiO\textsubscript{2}/Pt interface was increased in sputtered TiO\textsubscript{2} diode. The oxygen deficient state at TiO\textsubscript{2}/Pt interface generates Ti\textsuperscript{3+}, and these V\textsubscript{o} act as donor [2]. Therefore, the Fermi level of TiO\textsubscript{2} become closer to the conduction band when the increasing of the V\textsubscript{o}. As a result, SBH at TiO\textsubscript{2}/Pt interface is decrease, so the reverse current in sputtered TiO\textsubscript{2} diode is increase.

Fig. 4 shows the I-V characteristics of 1D-1R memory cell. The low resistance state (LRS) current (at 1/2V\textsubscript{Read}, cause the sneak current path) in the unselected cells was
largely suppressed in 1D-1R structure. This is because the sneak current through the unselected cells was effectively blocked by sol-gel TiO\textsubscript{x} oxide diode.

4. Conclusions

We reported a high on-off ratio and a stable rectification property in sol-gel processed Ti/TiO\textsubscript{x}/Pt structure diode. The rectifying property of sol-gel processed TiO\textsubscript{x} diode is better than that of sputtered TiO\textsubscript{2} diode. The oxygen vacancies at TiO\textsubscript{x}/Pt interface play important roles to reduce the reverse leakage current. By stacking the HfO\textsubscript{2} unipolar resistive memory cell on the sol-gel processed Ti/TiO\textsubscript{x}/Pt diode, the read disturbance from unselected cell was significantly reduced. Using the simple and cost-effective sol-gel processed TiO\textsubscript{x} diode device can make a high density memory array.

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References