Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials, Tsukuba, 2014, pp78-79

Improvement of Unipolar Resistive Switching by N_2 Annealing in Ni/ZrO_2/TaN Memory Device

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Abstract

The effects of the Ni/ZrO_2/TaN resistive switching memory devices without and with 400^o C annealing process were investigated. Due to a large amount of Ni diffusion, the device exhibits lower set and reset voltages after the annealing process. It also shows the excellent endurance which can be attributed to the less oxygen consumption in the period of reset process caused by the lower reset power.

1. Introduction

Nowadays, resistive random access memory (RRAM) has a lot potential of next generation memory because of its high density integration, high operation speed, low power consumption. In addition to ZrO_2, there is a lot variety of metal oxides materials to be used in RRAM, such as HfO_2 and NiO. Among the various materials of switching layer, ZrO_2 has become more and more popular with high dielectric constant, simple composition and semiconductor process compatibility. However, the issue of crossbar architecture for practical application is the crosstalk effect caused by sneak paths. To eliminate the crosstalk effect, 1D-1R (1diode-1resistor) structures with unipolar resistive switching (URS) are more simplified and better scalability than 1T-1R (1transistor-1resistor) structures with bipolar resistive switching [1]. In this point of view, the URS devices are more suitable for high density nonvolatile memory applications.

In the previous work, the devices show the stable and reproducible bipolar resistive switching (BRS) by introducing the interface between Ti and ZrO_2. We also demonstrated the ZrO_2 based devices with URS by inserting the metal nano-dots to enhance the effective electrical field [2] or constructing the double layers to form the different size of filament [3]. However, the investigation for the improvement of ZrO_2 based RRAM in URS behavior is still insufficient. In this work, we perform the Ni/ZrO_2/TaN device with the URS behavior. The high performance and high yield of the devices with URS behaviors by 400^o C post annealing (PA) process are demonstrated. The performance comparisons of the devices without and with PA for 30 min. are reported. We also depict the possible mechanisms of URS behavior in the Ni/ZrO_2/TaN device.

2. Device Fabrication

A 10 nm thick ZrO_2 film was deposited on TaN/Ta/SiO_2/Si substrate from a ZrO_2 ceramic target at 200^o C by an RF magnetron sputter. Subsequently, 20 nm Ni was fabricated by electron beam evaporation at room temperature as the top electrode (TE). Finally, a post annealing (PA) process at 400^o C for 30 min. in N_2 ambient was carried out. Electrical properties of the devices were measured by Agilent B1500A semiconductor parameter analyzer, where the bias voltage was applied on the Ni (TE) with TaN bottom electrode (BE) grounded.

3. Results and Discussion

Fig. 1 shows the cross-sectional TEM image of the Ni/ZrO_2/TaN memory device. There is TaON interfacial layer existed between ZrO_2 and BE. Figs. 2(a) and 2(b) reveal the typical RS behaviors in the Ni/ZrO_2/TaN devices without and with 400^o C annealing, respectively. Both the devices exhibit the unipolar resistive switching behavior but with the different V_{set}, V_{reset} and I_{reset}, as shown in Figs. 2(a) and 2(b). Fig. 3 is the statistical distributions of operation voltage (V_{set} and V_{reset}). This figure depicts that the mean values of V_{set} and V_{reset} dramatically decrease from 2.6 and 1.3 V to 1.6 and 0.6 V, respectively, after PA. The standard deviations of V_{set} and V_{reset} are also improved from 0.33 and 0.2 to 0.27 and 0.09, respectively. This large improvement of the operation voltage is attributed to the higher concentration of Ni diffusion into the ZrO_2 layer after PA which is confirmed by the depth profile of TOF-SIMS and XPS analysis in Figs. 4 and 5, respectively.

The LRS resistance of the device increases with an increase of temperature T as shown in Fig. 6, indicating that the conductive filament (CF) formed after set process is metallic-like. On the other hand, Fig. 7 shows the stable retention behavior at 150^o C of the annealed Ni/ZrO_2/TaN device up to 10^5s. The typical relaxation phenomena lead the HRS/LRS ratio is increased with the baking time [4]. As a result, we can construct the URS process in our devices based on Ni filament model as depicted in Fig. 8.

Moreover, the significant improvement is the endurance cycles of the device with PA. Figs. 9(a) and 9(b) are the endurance of the Ni/ZrO_2/TaN device without and with 400^o C annealing, respectively. The endurance is effectively improved to more than 1.5×10^4 cycles after PA process. That is because of the smaller reset current (I_{reset}) as shown in Fig. 10, leading the reset power (P_{reset}) of the Joule heating effect [5] in the URS devices is decreased after PA process. The device with PA takes the less power with the

smaller activation energy of oxygen ion migration during the reset process. As a result, the consumption of the movable oxygen ion could be minimized during every switching cycle. The switching endurance of the device can be largely improved.

4. Conclusion

In this work, the performance comparisons of $Ni/ZrO_2/TaN$ devices without and with PA are demonstrated. The URS mechanisms are also constructed. The switching properties of $Ni/ZrO_2/TaN$ devices including the mean values of operation voltages, variations of V_{set} and V_{reset} and endurance cycles are largely improved after PA process.

Acknowledgments

This work was supported by the National Science Council, Taiwan, under project NSC 102-2221-E-009-134-MY3.

References

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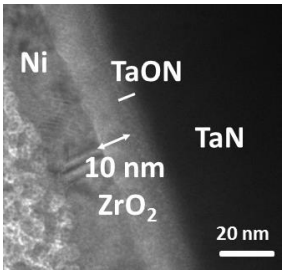

Fig. 1 Cross sectional TEM image of the $Ni/ZrO_2/TaN$ resistive switching memory device.

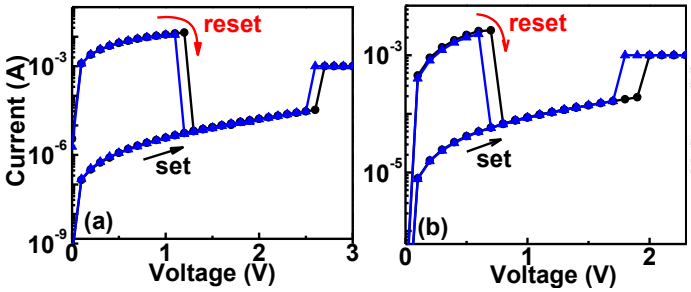

Fig. 2 Typical unipolar I-V switching curves of the $Ni/ZrO_2/TaN$ device without (a) and with 30 min. annealing (b).

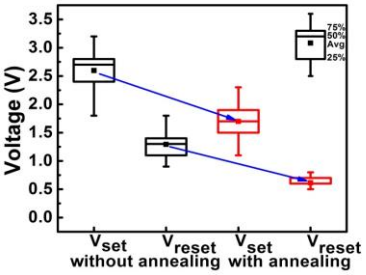

Fig. 3 Statistical distribution of set voltage and reset voltage.

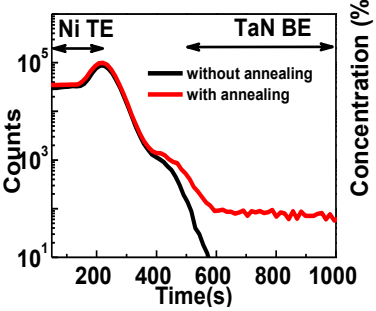

Fig. 4 TOF-SIMS profiles of Ni element in the $Ni/ZrO_2/TaN$ memory stack without and with PA.

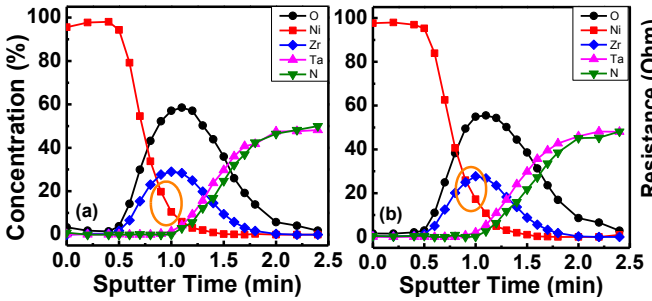

Fig. 5 XPS depth profiles of the $Ni/ZrO_2/TaN$ memory stack without (a) and with 30 min. annealing (b).

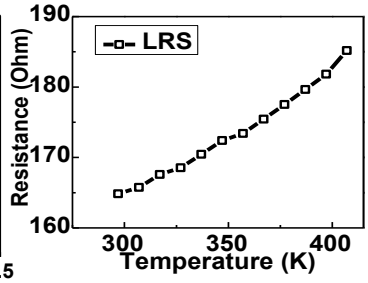

Fig. 6 Temperature dependence of the LRS resistance for the device with PA.

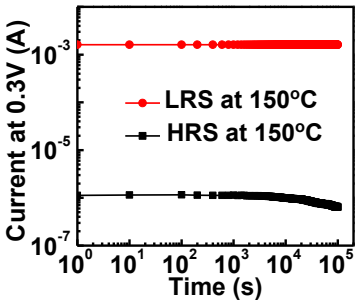

Fig. 7 Retention properties of the $Ni/ZrO_2/TaN$ device with PA at 150° C.

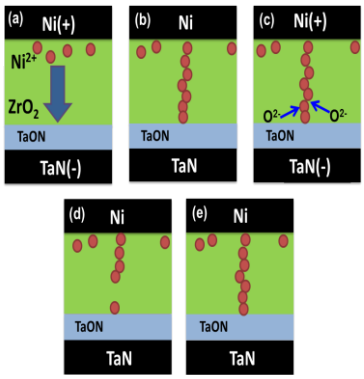

Fig. 8 Unipolar RS mechanism of the $Ni/ZrO_2/TaN$ memory stack with Ni filament.

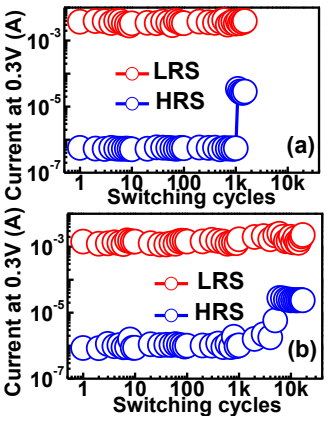

Fig. 9 The endurance characteristics of the devices without (a) and with PA process (b) for URS operation.

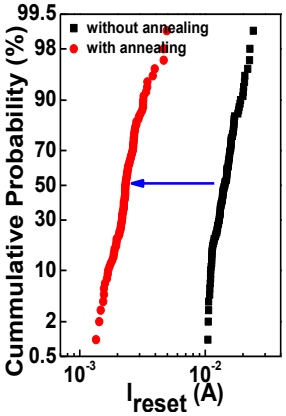

Fig. 10 Reset current distribution for 100 dc sweep cycles with different conditions.