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A Measurement of Ratio-less 12-transistor SRAM cell Operation at Ultra-low Supply-voltage

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Abstract

The ratio-less 12-transistor SRAM was developed and measured to evaluate the operation under ultra-low supply-voltage range. Its superior immunity to the device variability and its inherent operating ability at the supply voltage of 0.22V were experimentally confirmed.

1. Introduction

In the development of SRAMs for the deep sub-micron generation, it is difficult to maintain a sufficient operating margin in the conventional 6-transistor SRAM (6T-SRAM) cell, because of supply voltage scaling and device variability [1]. To overcome this problem, we proposed ratio-less 10-transistor SRAM [2] [3]. This enables the memory cell design that is free from consideration of the Static Noise Margin (SNM). It also enables stable SRAM function without the restriction of transistor parameter (W/L) settings in circuit design and the dependency on the device characteristic variation. Fig. 1 (a) shows the basic block diagram of the ratio-less SRAM (RL-SRAM) cell. In addition to the 6T-SRAM, the RL-SRAM cell has INV3 and SW3. The INV3 is the dedicated read buffer to drive the read bit-line while SW3 is added for breaking the flip-flop loop in the write operation. We have reported the basic ratio-less operation with the ratio-less 10-transistor SRAM cell in which the input switch and the output tri-state inverter was configured with single channels [2] [3]. However, for the low supply-voltage operation, it was suggested that the full complementary configuration of 12-transistor ratio-less cell as shown in Fig .1 (b) would be suitable.

In this paper, we developed the ratio-less 12-transistor SRAM (RL-12T-SRAM) test chip and measured to evaluate the operation at ultra-low supply-voltages.

2. Chip Design and Experimental Results

We designed 1Kbit SRAM TEGs in which both 6T-SRAM cells and RL-12T-SRAM cells are incorporated by using a 180nm CMOS process. The photos of developed chips are shown in Fig. 2. Fig. 3 shows the measured minimum operating supply voltage versus operating frequency obtained from the test with the marching pattern. For the 6T-SRAM, the minimum supply voltage is almost constant of 0.5V for the cycle time of 10[us] or more. On the other hand, the minimum supply voltage in RL-12T-SRAM reaches to 0.22V with the longer cycle time.

3. Comparison with the Simulated Result

Fig. 4 shows the circuit schematic that is used for the circuit simulation of Monte Carlo Analysis. Each MOS transistor in the memory cell has a voltage source at the gate terminal to shift its threshold voltage (Vth). Fig. 5 (a) (b) show the simulated results from the Monte Carlo analysis for 6T-SRAM and RL-12T-SRAM, respectively. As a result, if the Vth shift voltage is 20[mV] for one standard deviation, simulated results agree well with the measured results shown in Fig. 3. This means the minimum operating voltages for 6T-SRAM were strongly affected by the variability of transistors while the RL-12T-SRAM has a superior immunity to the device variability.

4. Fail Bit Distribution in Low Supply-voltage

Fig. 6 (a) (b) show the measured fail bit counts for the low supply-voltage at the low-frequency operation for 6T-SRAM and RL-12T-SRAM, respectively. As can be seen in these figures, the distribution of the supply voltage for 6T-SRAM between first failure bit and last failure bit is wider than that for the RL-12T-SRAM, especially in the low-frequency operation. This means a 6T-SRAM cell operation becomes more sensitive in low supply-voltage region. On the other hand, in RL-12T-SRAM, the failure bits occur nearly simultaneously even at low supply-voltage. This is because the basic operation of RL-12T-SRAM is the fully digital and complementary.

5. Conclusion

We have compared the measured results of minimum supply voltage between the developed RL-12T-SRAM and conventional 6T-SRAM. As a result, we confirmed that the RL-12T-SRAM has the strong immunity to the variability of device characteristics and the inherent ability of operation in ultra-low supply-voltage of 0.5V or less.

Acknowledgement

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References

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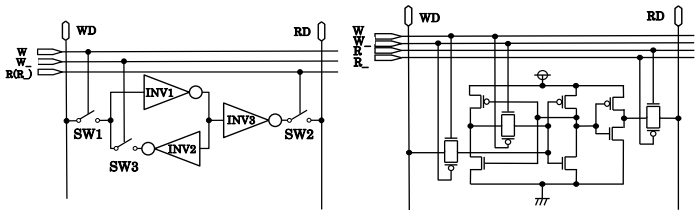
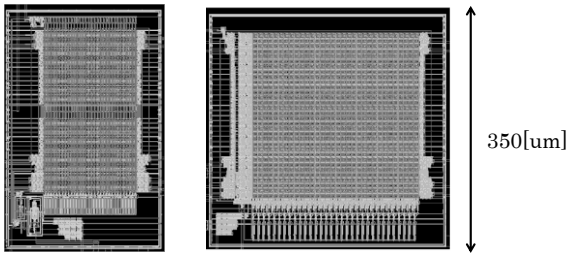
[2] T. Saito et al., "Ratio-less 10-Transistor Cell and Static Column Retention Loop Structure for Fully Digital SRAM Design" IEEE International Memory Workshop, vol.2012, pp.167-170, May 2012.

[3] H. Okamura et al., "Mosaic SRAM Cell TEGs with Intentionally-added Device Variability for Confirming the Ratio-less SRAM Operation" IEEE International Conference on Microelectronic Test Structure, pp212-215, Mar. 2013.



(a) Block diagram (b) Schematic

Fig. 1 Ratio-less 12T-SRAM



(a) 6T-SRAM (b) RL-12T-SRAM

Fig. 2 Chip Photograph

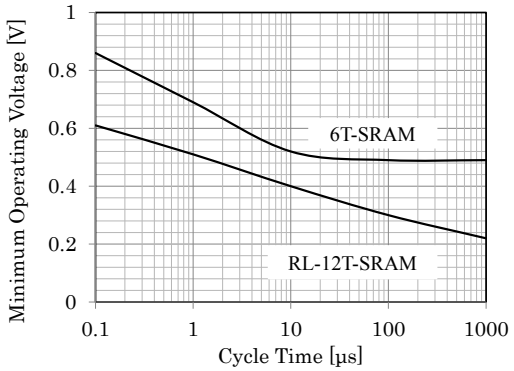


Fig. 3 Measured Minimum Operating Voltage versus Cycle Time

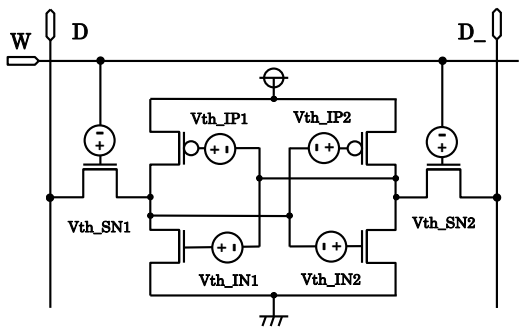
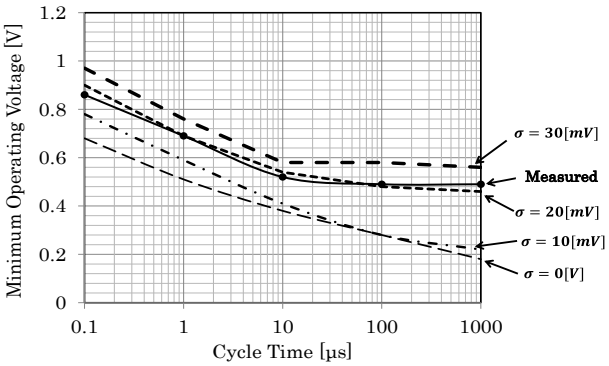
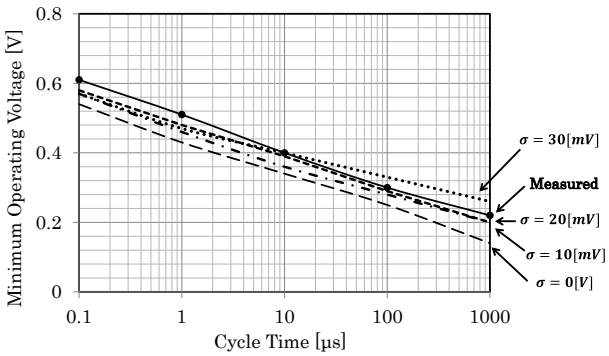


Fig. 4 Vth shift 6T-SRAM

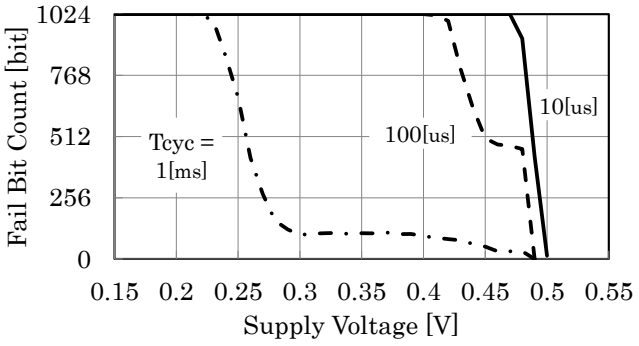


(a) 6T-SRAM

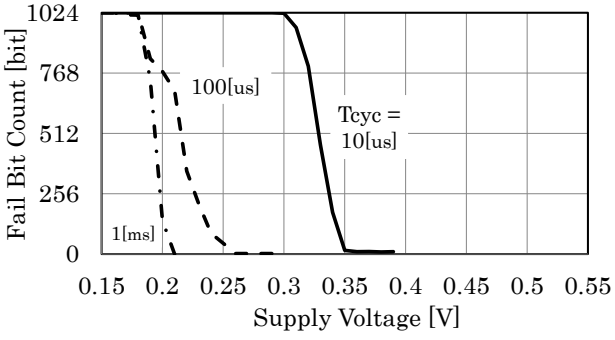


(b) RL-12T-SRAM

Fig. 5 Simulated Results of Monte Carlo Analysis



(a) 6T-SRAM



(b)RL-12T-SRAM

Fig. 6 Measured Fail bit Count versus Supply Voltage