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Enhanced Erasing Performance of Ω-Gate P-Channel Junctionless Fin-FET SOncOS Nonvolatile Memory

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I. Abstract

This work presents Ω-gate p-channel junctionless (JL) polycrystalline silicon (poly-Si) nanowires (NWs) nonvolatile memory (NVM) device with silicon nanocrystals (Si-NCs) charge trapping layer. Experimental results indicate that the p-channel device has better erasing efficiency. For p-channel device, an extrapolation of the memory window to 10 years demonstrates that the stored charge still retains 95 % of its initial value at high temperature of 85 ^{o}C. Such the Ω-gate p-channel JL-NVM is feasible for use in system-on-panel (SOP) and 3-D stacked flash memory applications.

II. Introduction

The concept of the junctionless (JL) field-effect transistor (FET) (JL-FET) device, which contains a single doping species at the same level in its source, drain, and channel, has received considerable attention recently [1]-[3]. The JL-FET structure is applied to a SONOS nonvolatile memory (NVM) with silicon nanocrystals (Si-NCs) that have also been investigated. Relatively few works have made a study of JL-FET NVM [4]-[6]. The comparison of programming/erasing (P/E) operation of p-channel JL-NVM has not been thoroughly elucidated. This work demonstrates the feasibility of using the P/E physical mechanism of Ω-gate p-channel JL SONOS NVM with Si-NCs (SOncOS). Additionally, the device reliability can be improved, owing to the property of the dispersed Si-NCs defects and its deep energy level.

III. Experiment

The Ω-gate JL SOncOS NVM was fabricated by initially growing a 40 nm-thick thermal oxide layer on 6 inch silicon wafers with a (100) orientation as substrates. A 50 nm undoped amorphous silicon (a-Si) layer was then deposited by low-pressure chemical vapor deposition (LPCVD) at 550 ^{o}C. Next, the a-Si layer was solid-phase recrystallized (SPC), subsequently forming a large grain size at 600 ^{o}C for 24 hrs in a nitrogen ambient atmosphere. Next, the p-channel device was implanted with BF_2 ions at a dose of 1×10^{14} cm^{-2}, and then activated at 600 ^{o}C for 4 hrs. The NW channels were patterned by electron beam (e-beam) lithography and then transferred by reactive-ion etching. Moreover, the devices were dipped in HF solution for 100 s to suspend the NWs. For forming the ultra-thin poly-Si NW channel, the naked NWs are firstly thermally oxidized, and then removing the first sacrificial oxide layer by HF dipping. After oxidation trimming process, the thickness of active layer is 14.5 nm. Next, thermal oxidation was performed to produce the tunnel oxide with a thickness of 2.5 nm, and final thickness of poly-Si is 12 nm. Additionally, 3 nm / 2 nm /3 nm of Si_3N_4 / a-Si / Si_3N_4 trapping layer were deposited by LPCVD, and then annealed at 1050 ^{o}C for 30 min in a nitrogen ambient atmosphere. A 10 nm-thick TEOS oxide layer was deposited as a blocking oxide. Additionally, 150 nm in-situ doped n^+ poly-silicon deposition was performed as a gate electrode and patterned by e-beam lithography and RIE. Moreover, a 200 nm SiO_2 passivation layer was deposited. Finally, 300 nm Al-Si-Cu metallization was performed and sintered.

IV. Results and Discussion

Fig. 1(a)-(b) schematic diagram of the Ω-gate p-channel JL SOncOS NVM. The details of the process flowchart of the fabricated devices are provided as well. Fig. 1(c)-(d) the top view SEM images of the Ω-gate p-channel JL SOncOS NVM with L_g = 1 μm. Fig. 2(a) shows the high-resolution transmission electron microscopy (TEM) image of a single NW of the Ω-gate JL SOncOS NVM. The poly-Si NW shows a rectangular shape, which is surrounded by n^+ poly-Si gate as a Ω-gate structure. Width and height of the NWs are 77 and 17 nm respectively [the effective width (W_{eff}) of the NW is 111 nm]. Fig. 2(b) shows the cross section of the hybrid layers and the diameter of the crystalline Si-NCs around 4 nm.

Fig. 3(a) and (b) describe the Fowerler–Nordheim (FN) programming and erasing characteristics of the Ω-gate p-channel JL SOncOS NVM (W_{eff} / L = 111 nm ×10 /1 μm), respectively. The device was programmed and erased by FN injection at V_g = 15 V and V_g = -21 V for 1s, respectively. The threshold voltage shifts (ΔV_{th}) of devices are 5.3 V and 4.8 V after the programming and erasing operation respectively. The ratio of ON/OFF currents of the device which was programmed and erased is approximately 10^8. Owing to the Ω-gate structure and ultra-thin channel, the gate control is excellent in terms of steep subthreshold slope (SS) and I_{on} / I_{off} controlling.

Fig. 4 shows the I_d-V_g curve of the endurance characteristic of the P/E cycles for the Ω-gate p-channel JL SOncOS NVM. This figure reveals a high I_{on}/I_{off} current ratio (> 10^8) after 10^4 P/E cycles. The programming and erasing condition are V_g=15V for 50 μs and V_g=-21V for 1 ms in the p-channel.

Fig. 5 shows the endurance characteristics of the Ω-gate p-channel JL SOncOS NVM with an initial ΔV_{th} of 2.5 V. This result reveals that every P/E cycle, there have no sufficient numbers of holes to compensate electrons in the trapping layer. For p-channel device, the ΔV_{th} exhibits a downward trend. This result also reveals that excess holes injection leads to over erasing. Notably, after 10^4 P/E cycles, the p-channel device has a higher ΔV_{th} of 2.5 V.

Fig. 6 shows the retention of the Ω-gate p-channel JL SOncOS NVM at a high temperature of 85 ^{o}C. For both p-channel device has an excellent retention (> 90 %) by extrapolation of the memory window after 10 years. Owing to the deep conduction and valence bands of the Si- NCs, most of the injected charge can be stored in Si-NCs or in the interface between Si-NCs and Si_3N_4. The trapped charges in Si_3N_4 can also be redistributed to Si-NCs by trap assisted tunneling at high temperature. Therefore, most of the stored charge can be concentrated in a deep level of Si-NCs.

Table I. compares the JL SONOS NVM with important parameters.

V. Conclusion

This work demonstrates the feasibility of the Ω-gate JL SOncOS NVM with for 3-D flash NVM. The Ω-gate p-channel JL SOncOS NVM exhibits a large ΔV_{th} and excellent retention. Moreover, p-channel device has better endurance due to its superior erasing efficiency. In short, this Ω-gate p-channel JL SOncOS NVM is suitable for future ultra-high density 3-D flash memory and embedded memory applications.

VI. References

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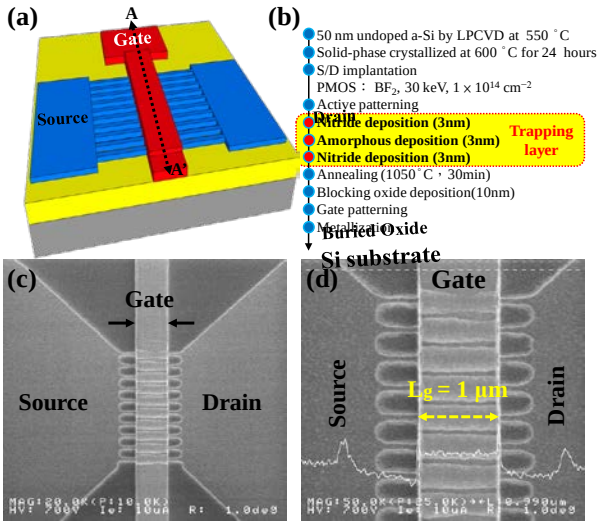

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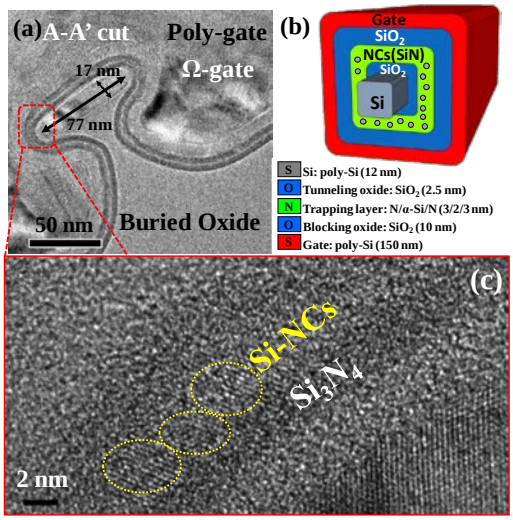

Fig. 2(a) TEM image of a single NW. (b) The Ω-gate p-channel JL SOncOS NVM, showing magnified the NW, thickness of each layer, and Si-NCs. (c) Magnified TEM image of the stacked SOncOS structure with Si-NCs (4 nm).

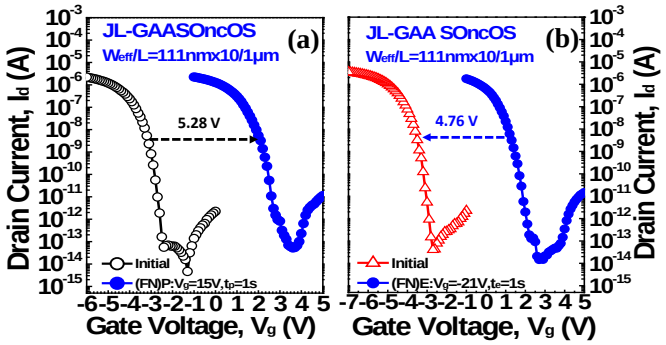

Fig. 3(a) FN programming, and (b) FN erasing hysteresis curves of the Ω-gate p-channel JL SOncOS NVM.

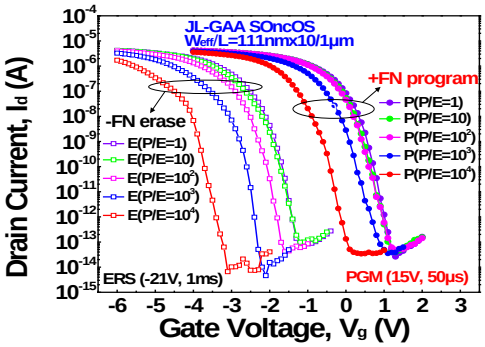

Fig. 4 P/E cycling endurance characteristics of the Ω-gate p-channel JL SOncOS NVM.

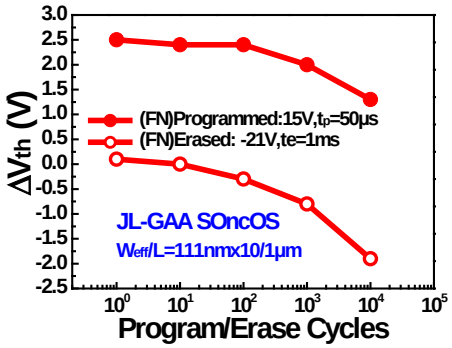

Fig. 5 Endurance characteristics of the Ω-gate p-channel JL SOncOS NVM.

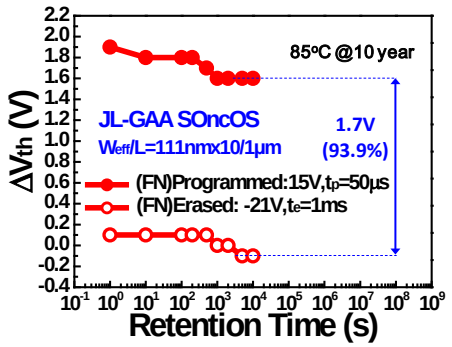

Fig. 6 Retention characteristics of the Ω-gate p-channel JL SOncOS NVM at 85 °C.

Table I
Lists important parameters in comparison with the other works

	This work	Ref.[A]	Ref.[B]	Ref.[C]	Ref.[D]
Tunnel Oxide (nm)	2.5	12	11	2.8	5
Storage layer (nm)	3/2/3	3/2/3	3/2/3	6.2	3
Block layer (nm)	10	12	19	7	7
NCs	W	W	W	W/O	W/O
Program Speed	5.28V,1sec @15V	4.2V,1sec @18V	9V,1sec @26V	3V,1sec @14V	4V,1sec @15V
Erase Speed	4.76V,1sec @-21V	5.2V,1sec @-23V	-9V,1sec @-29V	2.5V,1sec @-14V	2.5V,1sec @-15V

Ref. [A] M. F. Hung et al., APL, pp. 162108, 2011. Ref. [B] H. B. Chen et al., EDL, pp. 537, 2012. Ref. [C] S. J. Choi et al., EDL, pp. 602, 2011. Ref. [D] C. Y. Chen et al., EDL, pp. 602, 2011.