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A Dual-Mode Active Pixel Sensor for Low-Light-Level Detection Using a Hybrid Photodetector

Sanggwon Lee, Sung-Hyun Jo, Myunghan Bae, Byoung-Soo Choi, and Jang-Kyoo Shin

School of Electronics Engineering, Kyungpook National University
1370 Sankyuk-dong, Buk-gu, Daegu, 702-701, Korea
Phone: +82-53-950-5531, E-mail: jkshin@ee.knu.ac.kr

Abstract

This paper presents a dual-mode active pixel sensor (APS) for low-light-level detection using a hybrid photodetector (PD) in standard CMOS process. The proposed APS is composed of a gate/body-tied (GBT) PD for detecting low-light-level intensity and a conventional N-well/P-sub PD on the same focal plane. The four transistors of the proposed APS allow to have two modes: the photo-amplification mode for low-light level detection and the normal mode for higher image quality. The gain of the hybrid PD is a hundred-times larger compared to the conventional PD. Also, the dynamic range of the proposed APS is increased to 86 dB. Its pixel size is 10 μm^2 (fill factor: 51%) for testing pixel performance. The proposed APS is being fabricated by using 1-poly 6-metal 0.18 μm standard CMOS technology.

1. Introduction

CMOS image sensors (CISs) have several advantages such as low cost, low power, and easy integration with complex peripheral circuits. Basically, various photodetectors (PD) are available in stand CMOS process [1]. For examples, N+/P-well, P+/N-well, N-well/P-sub junction PD can be made by using the CMOS technology. The PD, however, suffers from low responsivity. To amplify the sensitivity of the PD, gate/body-tied (GBT) MOSFET-type PD have been embedded in standard CMOS process [2]. Although, the responsivity of the GBT active pixel sensor (APS) is improved compared to the conventional APS, it is difficult to apply to imaging applications due to very narrow dynamic range of the GBT APS.

In this paper, we propose a special method to improve the low-light-level sensitivity of the APS in standard CMOS process. The proposed APS is consisted of two PDs (GBT PD, N-well/P-sub PD) on the same region and four transistors for changing operation modes. In case of the low-light-level condition, a photo-transistor for amplifying is operated and in case of the normal light-level condition, conventional APS with N-well/P-sub PD is operated. Therefore, the proposed APS has better low-light-level sensitivity than that of the conventional APS.

2. Device and circuit structure

Fig. 1(a) and (b) show the symbol and cross-section of the hybrid PD, respectively. The photo-current (I_{ph_Normal}) is generated within the N-well/P-sub PD. At that time, the voltage of the N-well and gate is decreased because of the N-well/gate connection. Then, the photo-current ($I_{ph\_Amp.}$) is amplified due to the GBT PD [3]. Fig. 2(a) and (b) show the results of the simulation and measurement of the GBT PD with drain voltage as a function of photo-current and light power, respectively. The GBT PD allows for increasing the photo-current gain up to 10^2 as shown in Fig. 2. Fig. 3(a) shows the schematic of the proposed APS with a hybrid PD. The proposed APS is consisted of a hybrid PD (M1), switches for changing modes (M5, M6), a reset switch (M2), a source follower (M3), and a pixel selection switch (M4). The proposed APS has dual mode by controlling the switches (M5, M6). In normal mode, M5 is turned off first and M6 is turned on. At that time, the voltage of V_A is 0 V and FD node is connected to the N-well node. Second, FD node is resetted by V_{REF} of 1.8V. After the reset period, M2 is turned off and the voltage of the FD node is decreased because of the accumulation of electrons in N-well region. In photo-amplification mode, first, M5 is turned on and M6 is turn-off. At that time, the voltage of V_A is 1.8 V and FD node is connected to the drain of M1. The electrons are accumulated in the n-well region which decreases the gate voltage of M1 because of the N-well/gate connection, acting as a negative gate voltage. This mechanism significantly amplifies the photo-current of M1, as shown in Fig. 2. Fig. 3(b) shows the layout of the proposed APS. Its pixel size is 10 μm^2 for testing pixel performance. Fig. 4 shows the variation of the output voltage swing in each operation mode. The dynamic range of the proposed APS can be improved due to the hybrid PD. Fig. 5 shows the simulation results of the output voltage of the proposed APS with the photo-current in each operation mode. The photo-current of the proposed APS can be measured from 5 fA to 100 pA. From the simulation results, it is confirmed that the dynamic range of the proposed APS is increased to 86 dB.

3. Conclusions

In this paper, a dual-mode APS for low-light-level detection using a hybrid PD in standard CMOS process has been proposed. The proposed APS has a shared photodetection area with a GBT PD and an N-well/P-sub PD. Although the size of pixel is slightly larger than that of conventional 3-transistor APS, the proposed APS can detect light with at least two orders lower light intensity, as shown in Fig. 5. Therefore, the proposed APS might be useful in high-sensitivity image sensor applications.

Acknowledgements

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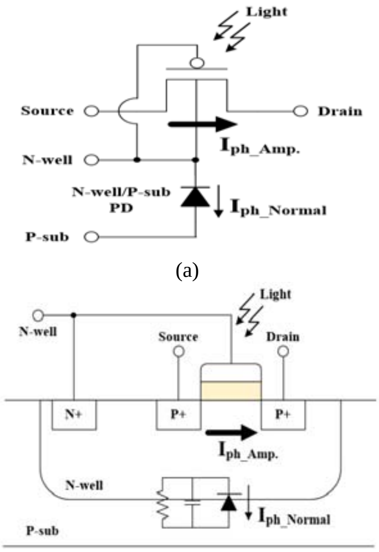

Fig. 1 (a) Symbol and (b) cross-section of the hybrid PD.

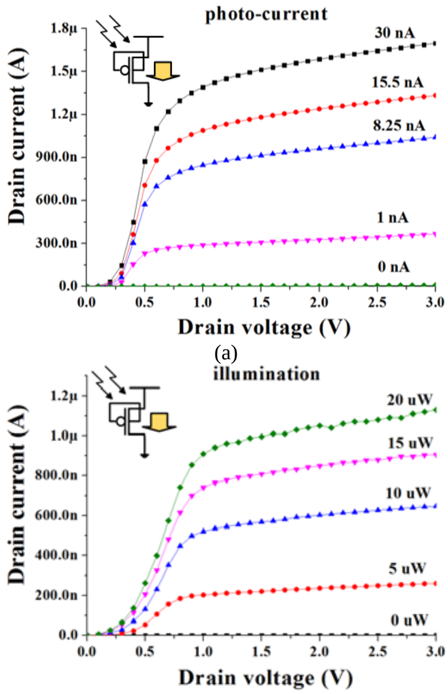

Fig. 2 (a) Simulation and (b) measurement results of the GBT PD with drain voltage as a function of photo-current and light power.

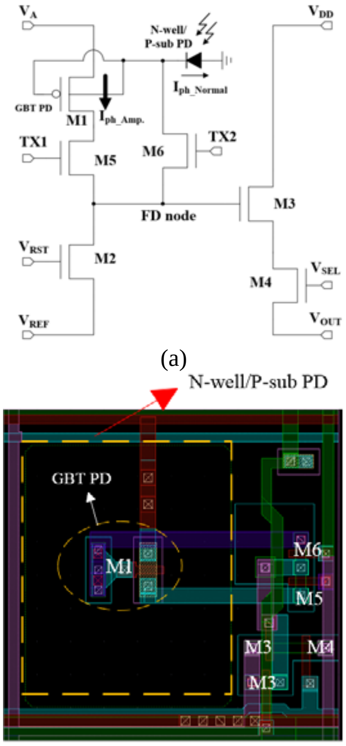

Fig. 3 (a) Schematic and (b) layout of the proposed APS.

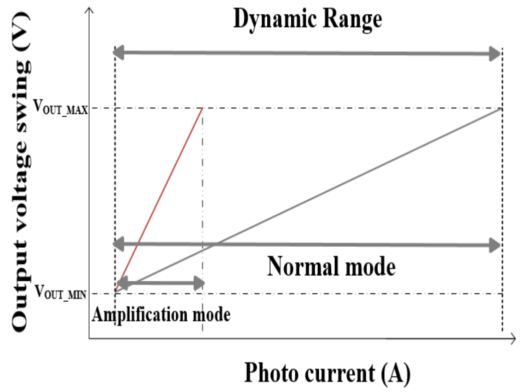

Fig. 4 Variation of the output voltage swing in each operation mode.

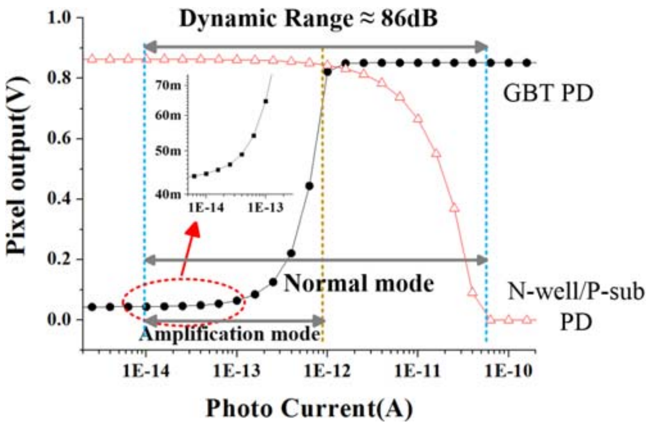

Fig. 5 Simulation results of the proposed APS output voltage with the photo-current in each operation mode. The inset shows pixel output of amplification mode from 5 fA to 100 fA.