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Diode Modeling with Lossy Nonlinear Capacitance Model

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1. Introduction

MOSFET models in a circuit simulator should have predictive power in DC I-V characteristics and RF small- and large-signal characteristics to estimate circuit characteristics including power consumption precisely [1-3]. By using the MOSFET model built only from small-signal measurement data, however, measured and simulated large-signal circuit characteristics often show considerable discrepancy. To realize an accurate model, it is necessary to establish a physically-consistent nonlinear model [4] from the result of the small signal measurements. Although a small-signal model from the S-parameters can be easily established [5-8], it may become physically inconsistent as a nonlinear model. In this paper, a physically-consistent lossy nonlinear model is proposed for the pn-junction diode in a silicon substrate, which is derived from the results of S-parameter measurements. A pn diode is modeled as combined nonlinear capacitor and resistor extracted from measured voltage-dependent small-signal characteristics from DC to 60 GHz with 65nm CMOS process. The diode model is expected to realize a predictive MOSFET model for both small- and large-signal characteristics.

2. Lossy Nonlinear Model Using Multi-Terminal Dvice

Figure 2 shows a small-signal equivalent circuit of an MOSFET and gate-to-source bias-voltage dependences of extracted small-signal input capacitance and resistance. When we consider lossy capacitor with no DC leakage current, capacitance and resistance should be connected in series in the equivalent circuit. When the bias voltage is applied at two terminals in the lossy capacitor, the bias-dependent capacitance and resistance should be considered as three-terminal devices with control terminal as shown in Fig. 3(a). Here, it is assumed that the charge in capacitor and current in resistor are proportional to the voltage across the device since the intermediate node of series capacitor and resistor is unknown. On the other hand, capacitance and resistance are changed nonlinearly by controlled voltages.

When the bias-dependent lossy capacitor is used in a two-port circuit, it is considered as a four-terminal device as shown in Fig. 3(b). In this case, physical consistency in the device has to be also considered in a nonlinear model. In other words, charge in nonlinear capacitor and current in nonlinear resistor should be described by continuous functions of multi-control voltages. Figure 4 shows a schematic view of bias-dependent nonlinear charge. Two measured small-signal capacitances correspond to orthogonal differential values on a charge surface. Therefore, a charge function is synthesized by merging the equivalent circuits for Y12 and Y11 (or Y21 and Y22). As a result, the topology of the nonlinear equivalent circuit can be determined if the small-signal topologies of Y12 and Y11 (or Y21 and Y22) are same. To realize the continuous functions, the virtual charge Q^* in a nonlinear capacitance and virtual current I^* in a nonlinear resistance are considered by the surface integration of the small-signal capacitance and resistance, respectively. Although the integration can be applied when the small-signal values are obtained densely, the integrated results are also obtained by assuming the function of the charge and the current even when the number of small-signal values is limited. In this case, the parameters in the function are extracted by comparing the differentiated function and measured small-signal parameters as

$$\frac{\partial I^*(V_1,V_2)}{\partial V_1} = g_1(V_1,V_2), \frac{\partial I^*(V_1,V_2)}{\partial V_2} = g_2(V_1,V_2),$$

$$\frac{\partial Q^*(V_1,V_2)}{\partial V_1} = c_1(V_1,V_2), \frac{\partial Q^*(V_1,V_2)}{\partial V_2} = c_2(V_1,V_2) \quad (1)$$

Finally, charge in nonlinear capacitor and current in nonlinear resistor are calculated as

$$\mathrm{I_R}(V_1,V_2,V_c) = V_R\left(\frac{\partial I^*}{\partial V_1} + \frac{\partial I^*}{\partial V_2}\right)(V_1,V_2)$$

$$\mathrm{I_R}(V_1,V_2,V_c) = V_R\left(\frac{\partial I^*}{\partial V_1} + \frac{\partial I^*}{\partial V_2}\right)(V_1,V_2) \quad (2)$$

Figure 5 shows the small signal equivalent circuit and a nonlinear circuit of a pn junction diode fabricated with 65nm CMOS process. Fig. 6 is a comparison of the simulation results of the model was generated using the proposed method and the measurement results of the pn junction diode fabricated. Scattering parameters measured is found to have changed by the bias. Simulated S parameters using the nonlinear model proposed in this paper and measured S parameters are compared.

3. Conclusions

In this paper, we proposed the physically-consistent nonlinear lossy capacitor model by using multi-terminal devices. The proposed model is described by combining a nonlinear resistor and nonlinear capacitor controlled with virtual current and charge surfaces by integrating small-signal conductance and capacitance obtained from the results of small-signal measurements, respectively. The proposed nonlinear model was verified by the pn junction diode fabricated with 65 nm CMOS process.

Acknowledgements

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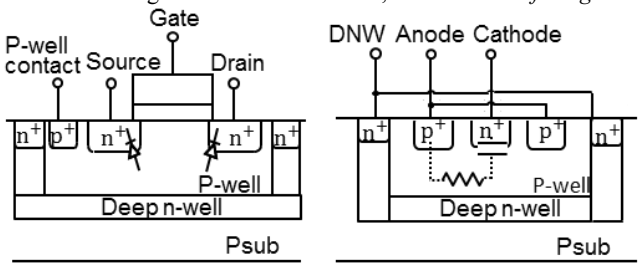
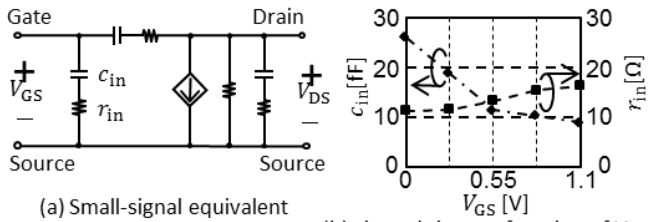


(a) MOSFET of triple-well structure.

(b) Test device for pn-junction diode for the MOSFET.

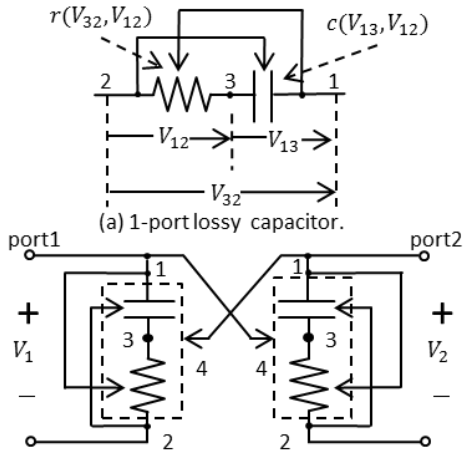
Fig. 1. Cross-sectional views.



(a) Small-signal equivalent circuit of the MOSFET.

(b) cin and rin as a function of Vgs

Fig. 2. Small-signal equivalent circuit of the MOSFET and bias-voltage dependences of cin and rin from measurement results.



(a) 1-port lossy capacitor.

(b) 2-port lossy capacitor.

Fig. 3. Equivalent circuit s of a lossy capacitor using multi-terminal elements.

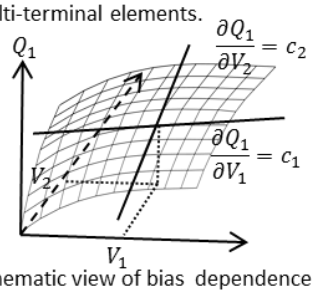
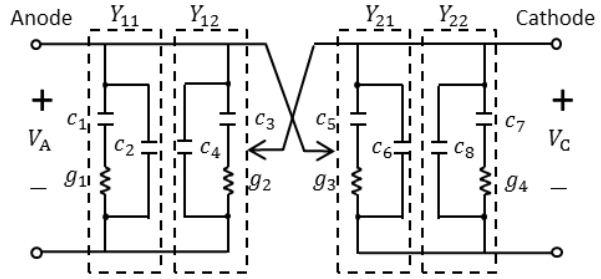
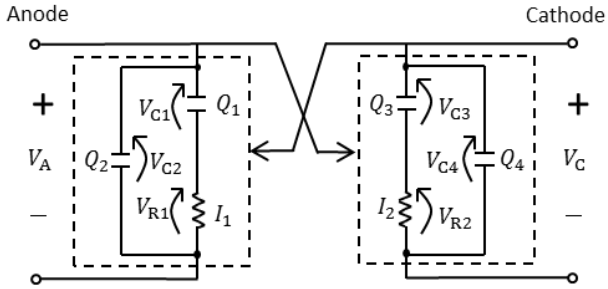


Fig. 4. Schematic view of bias dependence of the charge of nonlinear capacitor.



(a) Small-signal 2-port nonlinear lossy capacitor



(b) Large-signal 2-port nonlinear lossy capacitor

Fig. 5. Equivalent circuits of nonlinear model of the pn-junction diode.

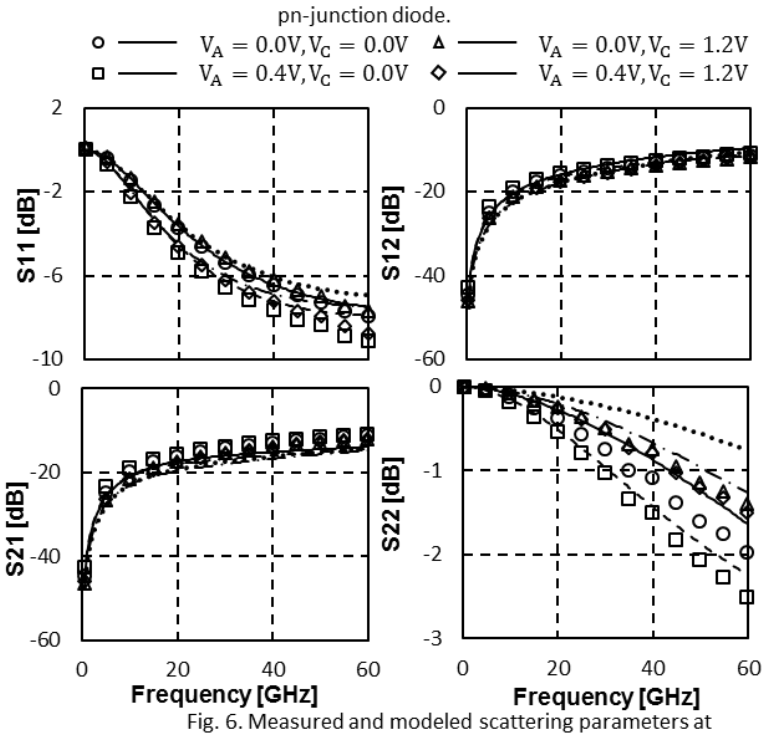


Fig. 6. Measured and modeled scattering parameters at various biases a function of frequency.