Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials, Tsukuba, 2014, pp108-109

A high-frequency level-up shifter based on 0.18μm vertical MOSFETs with more than 70% reduction of overshoot-voltage above VDD

Satoru Tanoi[1,2], and Tetsuo Endoh [1,2]

[1] Center for Innovative Integrated Electronic Systems, Tohoku University. [2] ACCEL, JST
468-1 Aramaki aza Aoba 6-6-0, Aoba-ku, Sendai 980-0845, Japan.
Phone: +81-3-5549-6909 E-mail: endoh@cies.tohoku.ac.jp

Abstract

A high frequency and high reliable level-up shifter is proposed. In the design, an initialize circuit, a voltage limiter and a dynamic biasing feed-back are added. In the simulation, our circuit based on 0.18μm vertical MOSFETs shows more than 70% reduction of the overshoot voltages above V_{DD} from the conventional. It achieves 164-MHz operation frequency with 2-pF loads at 1.8-V maximum voltage applied to the MOSFETS, which is larger than 1.6 times of the conventional frequency.

1. Introduction

Recently, many high-voltage tolerant level-up shifters using the thin-film MOSFETs for low V_{DD} have been developed for high frequency-switching in the power management systems[1]. Though the circuit is comparatively fast with high V_{DD}, the speed rapidly decreases as V_{DD} decreases. Thus, the further speed-advanced circuit has also reported[2]. In the circuit, however, the large overshoot voltages above V_{DD} are applied to the MOSFETs. To be overcome the problems, a new level-up shifter based on the vertical MOSFETs[3] with the dynamic biasing feed-backs is proposed. This paper describes our design and the excellent features.

2. Design for Overshoot Voltage reduction

Figure 1(a) and (b) show the conventional speed advanced level-up shifter[2] and our proposed one relatively. The input voltage swing between V_{DD} and 0V is converted to the swing between 2x V_{DD} and V_{DD} at Q, Qb. In our design, a voltage limiter VL(Fig. 1 (c)), a dynamic biasing feed-back BD(Fig. 1(d)), and $N_{2l,}$ N_{2r} are added for the overshoot voltage reduction. INIT is initialize circuit. The overshoots arise at the output falling. Figure 2 shows the voltage waveforms in each circuit at the output falling. In the conventional, the level of Yb falls rapidly and Qb falls slow. Therefore, the large voltages(>>V_{DD}) are applied to the MOSFETs P_{2l}, P_{1l} at Qb falling. In our circuit(Fig. 2(b)), Vgs of P_{2l} is small enough, because of the voltage limiter. INIT, P_{a5} and N_{a2} pre-charge to QG(QGb) at Q (Qb) rising. Thanks to the dynamic biasing feed-back, YGb becomes high-Z at Qb falling and the level drops momentary. Thus, Qb fall-time tf is reduced. Since Qb rapidly falls, the Vds overshoot of P_{1l} is suppressed. Furthermore, $N_{2l,}$ N_{2r} share the voltage drops.

3. Simulations

For the simulations, 0.18μm planar MOS parameters (typical) are used. The vertical MOSFET with the large Φ (around 0.18μm) can be approximated by the planar models without the back-bias effect[3]. Using the multi-pillar body-isolated vertical MOSFETs[3-4] shown in Fig. 3(a), the turn-on current I_b by the well-parasitic diode can be removed. Thus, JS of MOSFET models is set as zero(Fig. 3(b)). The gate width W_0 of a MOSFET pillar is set as 560nm (Φ=0.178μm) and number of pillar for each MOSFET is tuned for I_{ds} tuning as shown in Table. I.

The relations between the maximum voltages V_{gsmax}, V_{gdmax}, V_{dsmax} of the MOSFETs and number of pillar m_{p2} (for P_{2l}, P_{2r}) are shown in Fig. 4. The data with 3% or more overshoots are plotted. In the conventional, V_{gsmax}(or V_{gdmax}) overshoots above V_{DD} and V_{dsmax} one are larager than 0.62V, and 0.65V respectively. The overshoots of V_{gsmax}(or V_{gdmax}) and V_{dsmax} in our circuit are 0.08V(>87% reduction) and 0.16V(>75% reduction) respectively. The relations the maximum voltages to MOSFETs between and number of pillar m_{p1} (for P_{1l}, P_{1r}) are shown in Fig. 5. The conventional V_{gsmax}(or V_{gdmax}) overshoots and V_{dsmax} one are larger than 0.63V, and 0.66V respectively. Those of V_{gsmax} (or V_{gdmax}) and V_{dsmax} in our circuit are 0.08V(>87% reduction) and 0.19V(>71% reduction) respectively. Thus, the overshoot voltages of our circuit are reduced by 70% or more from the conventional.

Figure 6 shows the output rise time tr, the fall time tf and the power consumption P_{ower} in the conventional and the proposed. tr of the conventional is about same as that of the proposed. When m_{p2} increases, tf of the conventional decreases. tf of the proposed is about flat to m_{p2}. This reason is the main discharge-path difference; the paths of the conventional are P_{2l}, P_{2r} and those of the proposed are P_{1l}, P_{1r}. In the simulations, the speed optimized m_{p1} for the conventional and our proposed are 8 and 2 relatively.

The trade-off relations between the maximum voltage V_{MOSmax} applied to all MOSFETs voltages and the operation frequency f_{max} in the conventional and our circuit are shown in Fig. 7(a). The optimized m_{p1} for each circuit is used. f_{max} is calculated from tr and tf. Our circuit shows the highest frequency with the same V_{MOSmax}, and achieves 164MHz with 2-pF loads and 1.8-V V_{MOSmax}, which is larger than 1.6 times of the conventional[2]. The relations between the power consumption and f_{max} are shown in Fig. 7(b). The reverse current to V_{DD} is ignored. In P_{ower}-f_{max} trade-off, our circuit is very advantageous to the conven-

tional[1] and is about same as the conventional[2].

4. Conclusions

The level-up shifters with applied voltage limiting is proposed. The circuit is designed using vertical MOSFET without the well-diode turn-on. In the simulations, the proposed circuit reduces the overshoot voltages above V_{DD} by 70% or more from the conventional, and achieves 164MHz at 1.8-V maximum voltages applied to MOSFETs, which is larger than 1.6 times of the conventional frequency.

Acknowledgements

This work has been supported in part by JST, ACCEL. This work was designed in with Cadence and Synopsys tools, and in the chip fabrication program of VDEC, the University of Tokyo in collaboration with Rohm.

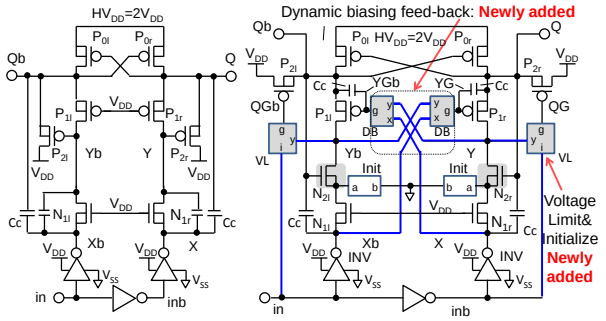
References

[1]S. Rajapandian, et al., IEEE J. Solid-State Circuits, **41** (2006) 1400.

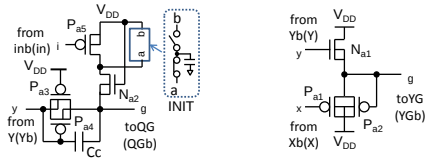
[2]C. Huang and H. Lin, Jpn. J. Appl. Phys. **51** (2012) 02BE08.

[3]K. Sakui and T. Endoh, IEEE ICMTS, Proc. (2010) 220.

[4]T. Endoh, et al., IEICE Trans. Electron., E93-C, (2010) 557.

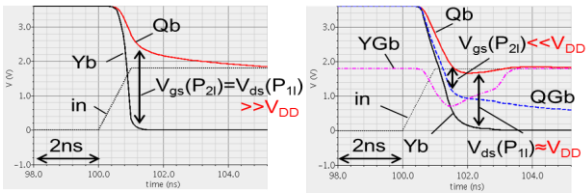


(a) Conventional[2] (b) Core of proposed



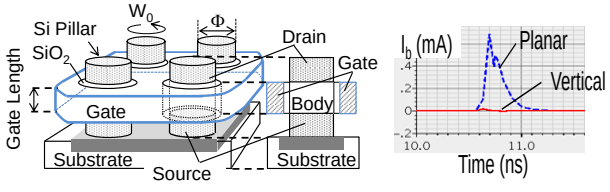
(c) Voltage limiter VL withINIT. (d) Dynamic biasing DB

Fig.1 Level-up shifter of conventional and proposed.



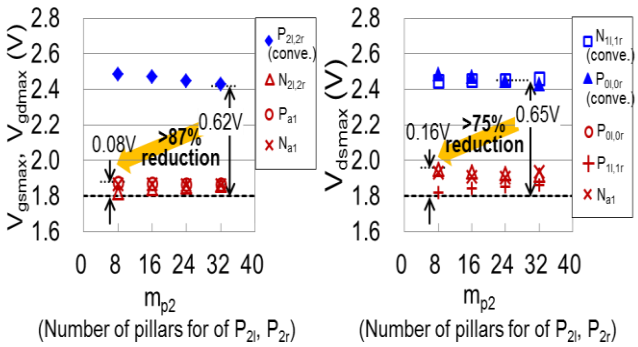
(a) Conventional[2] (b) Proposed

Fig. 2 Voltage waveforms at output falling.



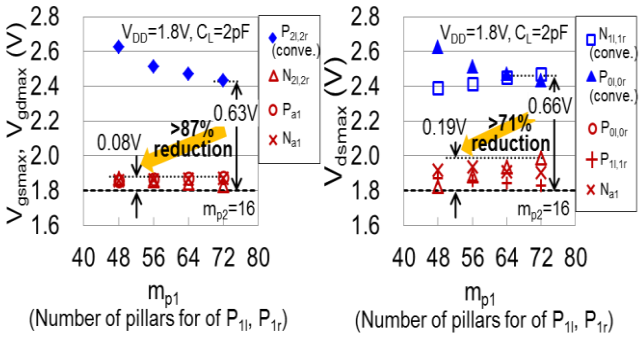
(a) Structure[3][4] (b) I_b waveforms

Fig. 3 Structure and Ib of Vertical MOSFET.



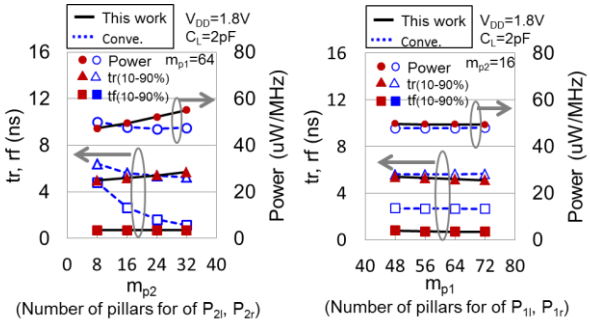
(a) Maximum Vgs, Vgd (b) Maximum Vds

Fig. 4 Relations between m_{p2} and Maximum voltages to MOSFETs.



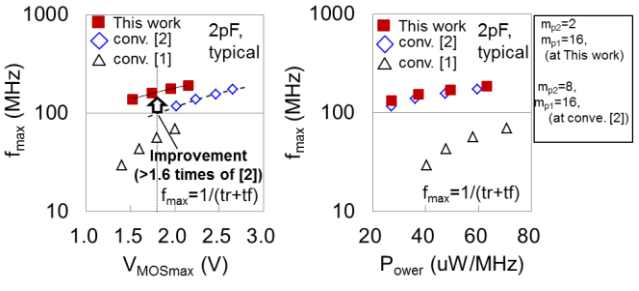
(a) Maximum Vgs, Vgd (b) Maximum Vds

Fig. 5 Relations between m_{p1} and Maximum voltages to MOSFETs.



(a) m_{p2} vs tr, tf (b) m_{p1} vs tr, tf

Fig. 6 Relations between m_{p2}, m_{p1} and tr, tf.



(a) V_{mosmax} vs f_{max} (b) Power vs f_{max}

Fig. 7 Trade-off relations(V_{mosmax} vs f_{max} and P_{ower} vs f_{max}).

Table. I Number of Pillars for each MOSFET's.

	Variables		Constants					
symbole in Fig. 1	P_{1l}, P_{1r}	P_{2l}, P_{2r}	P_{0l}, P_{0r}	N_{1l}, N_{1r}	N_{2l}, N_{2r}	P_{aj} (j=1,2..)	N_{aj} (j=1,2..)	NMOS in INV
Number of Pillars	m_{p1}	m_{p2}	8	24	48	4	2	24
Range	8 to 32	48 to 72						