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Comparison of Power Gain Performance between Conventional and Independently Biased HBT Cascode Chips

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Abstract

This paper aims to study power gain performance of independently biased cascode structure in comparison to that of conventional one at 1.9 GHz band by employing a monolithic microwave integrated circuit (MMIC) InGaP/GaAs heterojunction bipolar transistor (HBT) cascode chip. It is found that proposed cascode structure can deliver superior power gain performance over conventional one by setting appropriate bias conditions.

1. Introduction

Cascode circuit cascading the first common-emitter transistor and second common-base transistor which is first proposed by W.B. Shokley in 1949 [1] can deliver a number of advantages such as wide bandwidth, high frequency characteristics, high isolation between input and output and high gain due to reduction of Miller effect and high isolation of cascading structure. However the conventional cascode structure encounters an issue of instability of DC operating between two transistors due to its floating potential. In order to overcome this issue, new cascode circuitry has been proposed by inserting an added bias terminal to the common point between two transistors [2] resulting in an ability of setting independently biased condition for each individual transistor and better power efficiency and linearity characteristics over conventional cascode structure [3]. Nevertheless power gain characteristic of this new cascode structure has never been studied, thus purpose of this study is to discuss and clear power gain performance of the new cascode structure to conventional one under investigation of the optimum bias conditions to obtain superior power gain performance of new cascode structure.

2. Bias conditions analysis

Conventional and proposed cascode circuitries are depicted in Fig. 1 in which floating point is stuck in the mid-point between two transistors for the case of conventional cascode structure whereas an added bias terminal is inserted to the mid-point between two transistors in case of proposed cascode structure. These cascode configurations can be approximated with a simple mall-signal equivalent circuit as a two-port network as illustrated in Fig. 2 where g_m, g_0, g_π denote conductance values at a given bias point. For a proper comparison in power gain between conventional and new cascode structures, input power is set the same for both of them, hence from the small-signal equivalent circuit, it can be concluded that the difference in power gain between new and conventional cascode structures is determined by the difference in second-stage transistor's collector bias terminal (I_{c2} or V_{cc2}) between them since this bias terminal relates to output resistance of cascode circuit which in turn defines the maximum power gain through eq. (1):

$$r_0 = \frac{v_3}{i_{c2}}\Big|_{v_1=0} \approx \frac{1}{g_{02}}\left(1+\frac{g_{m2}}{g_{\pi 2}}\right) \tag{1}$$

Providing that $g_{m2} >> g_{02}$ and $g_{\pi 2} >> g_{01}$. Using static IV characteristic formulas of bipolar junction transistor (BJT) and taking small-signal approximations to derive expressions of g_m, g_0, g_π:

$$I_c = I_S \exp\left(\frac{V_{be}}{V_T}\right)\left(1+\frac{V_{ce}}{V_A}\right) \rightarrow g_0 = \frac{\partial i_c}{\partial v_{ce}} \approx \frac{I_c}{V_A} \tag{2}$$

$$I_c = I_S \exp\left(\frac{V_{be}}{V_T}\right)\left(1+\frac{V_{ce}}{V_A}\right) \rightarrow g_m = \frac{\partial i_c}{\partial v_{be}} \approx \frac{I_c}{V_T} \tag{3}$$

$$I_b = I_{Bo} \exp\left(\frac{V_{be}}{V_T}\right) \rightarrow g_\pi = \frac{\partial i_b}{\partial v_{be}} \approx \frac{I_b}{V_T} \tag{4}$$

$$V_T = \frac{kT}{q}$$

where V_A and V_T are Early voltage and thermal voltage respectively and I_c, I_b are the DC bias currents. Substituting (2) - (4) into (1), it is seen that the output resistance r_0 is mainly affected by I_{c2}. From that, two investigations as shown in Fig. 4 and Fig. 5 are conducted based on static IV characteristic of cascode configuration indicated in Fig. 3, to deal with further the role of bias terminals, especially I_{c2} to power gain difference between two cascode structures. As can be seen in Fig. 3, for conventional cascode structure because the same collector bias current flows through two transistors, one of two transistors is forced to be biased in saturation region, so the other must be biased in active region, which is indicated with stable bias points Q_1 and Q_2, as a result bias point cannot be set independently. However for proposed cascode one, owing to the added bias terminal, bias point for each transistor is able to set independently. In the first bias scenario at high V_{cc2} described in Fig. 4 with two transistors of new cascode structure biased in active region, I_{c2n} is always higher than I_{c2c} resulting in better power gain performance of new cascode structure. On the other hand, in the second bias scenario at low V_{cc2} in Fig. 5 with second transistor in saturation mode and first transistor in active mode, I_{c2n} varied with the variation of V_{cc1} can be higher or lower than I_{c2c}, consequently power gain of new cascode structure can be better or poorer than that of conventional cascode one depending on V_{cc1}. It is noted in these investigations that total collector bias voltage V_{cc} and base bias current I_b are kept the same for both types of

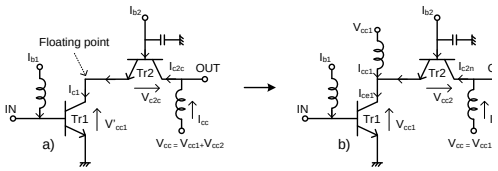

Fig.1 Cascode structure: a, Conventional b, Proposed

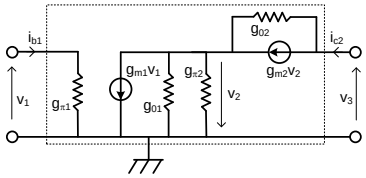

Fig.2 Small-signal equivalent circuit

Table.1 Bias conditions

Bias	Unit	First investigation		Second investigation	
		Exp.	Sim.	Exp.	Sim.
I_b	mA	0.12	0.11	0.30	0.28
V_{cc1}	V	1.0 ÷ 3.0	1.3 ÷ 3.3	1.5 ÷ 5.5	1.66 ÷ 5.58
V_{cc2}	V	4.0	3.7	0.44	0.36

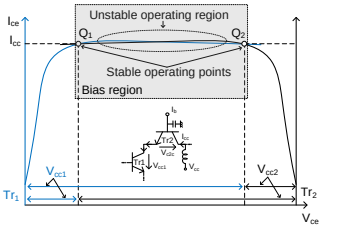

Fig.3 Bias condition of conventional cascode structure with two stable bias points Q_1 and Q_2 where one of two transistors is forced to be biased in saturation region, so the other must be biased in saturation region. In other words, bias point cannot be set independently.

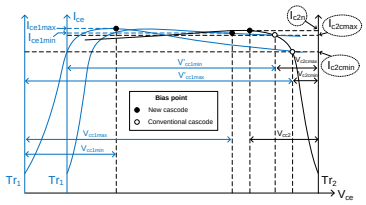

Fig.4 First analysis at high V_{cc2} on static IV characteristic. New cascode with both two transistors operated in active mode shows higher second-stage collector bias current I_{c2} than that of conventional one with bias condition of having one transistor in saturation region.

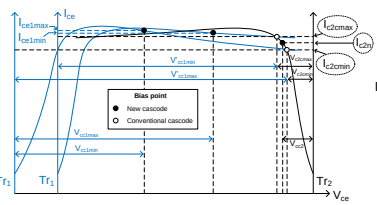

Fig.5 Second analysis at low V_{cc2} on static IV characteristic. New cascode structure with bias condition similar to that of conventional cascode one with one transistor operated in saturation mode can show higher or lower second-stage collector bias current I_{c2} than that of conventional one due to the variation of V_{cc1}.

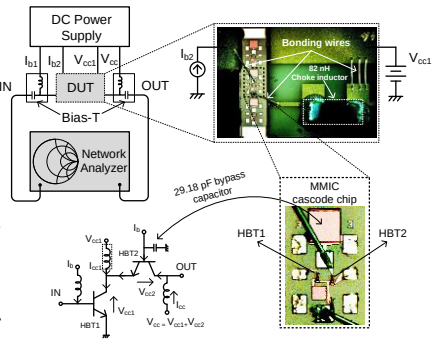

Fig.6 Experimental setup

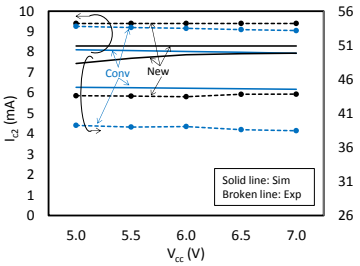

Fig.7 First investigation of bias condition on power gain at high V_{cc2} and low I_b

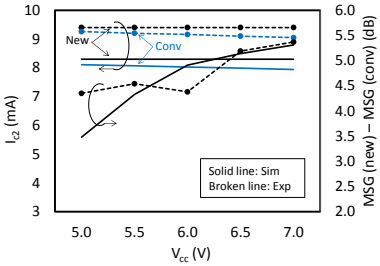

Fig.8 First investigation of bias condition on power gain difference at high V_{cc2} and low I_b

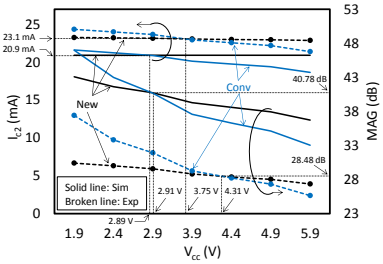

Fig.9 Second investigation of bias condition on power gain at low V_{cc2} and high I_b

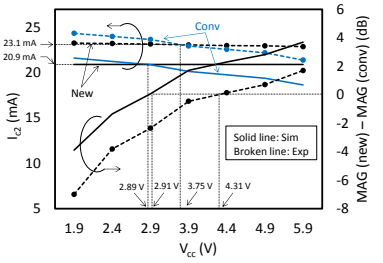

Fig.10 Second investigation of bias condition on power gain difference at low V_{cc2} and high I_b

cascode structures. After setting optimum value for V_{cc2} obtain higher I_{c2}, thus better power gain performance for new cascode structure, V_{cc1} then should be increased to make this better power gain much higher. This is because increasing V_{cc1} results in the decrease in I_{c2c} as total collector bias voltage V_{cc} remains the same for both types of cascode structures as clearly seen in the Fig. 4 and Fig. 5.

3. Results

Experimental setup

Figure. 6 describes experimental setup for measuring S-parameters of conventional and new MMIC HBT cascode chips at 1.9 GHz band to calculate their maximum available gain (MAG) and maximum stable gain (MSG). The cascode chip is composed of two InGaP/GaAs HBTs with the same size of 2 μm × 20 μm × 2 fingers. Since two transistors have the same size, base bias current is set equally for them (I_{b1} = I_{b2} = I_b) to avoid undesired impacts. This means base current doesn't contribute to power gain of cascode structure and it is not dealt with in the investigations. In addition, to confirm the bias analysis on power gain difference discussed in Sec. 2, second-stage collector bias voltage V_{cc2} is kept at high and low values whereas the first-stage or added bias voltage V_{cc1} is allowed to vary and total collector bias voltage V_{cc} remains the same for both types of cascode structures.

Bias conditions investigation

Bias conditions for two investigations at high and low V_{cc2} are shown in Table. 1 where first investigation is conducted at high V_{cc2} and low I_b and second investigation is conducted at low V_{cc2} and high I_b. Results of these two investigations which aim to confirm what are discussed in Sec. 2 are illustrated in Fig. 7 – Fig. 10. As seen in Fig. 7 and Fig. 8, both simulation and experiment indicate that power gain performance (MSG) of new cascode structure is always better than that of conventional one due to its higher second-stage collector bias current (I_{c2}). However results in Fig. 9 and Fig. 10 show that at low V_{cc2}, whether I_{c2n} is higher or lower than I_{c2c} depends on V_{cc1}, consequently power gain performance (MAG) of new cascode structure can be higher or poorer than that of conventional one depends on V_{cc1}. The contribution of V_{cc1} to power gain difference can be clearly seen in Fig. 8 and Fig. 10 where it shows that the higher V_{cc1}, the higher I_{c2n} compared to I_{c2c}, thus the better power gain of new cascode structure compared to conventional one. These conclusions agree with the findings discussed in Sec. 2 on bias conditions.

4. Conclusion

This study has demonstrated that by setting appropriate bias condition, independently biased HBT cascode structure can offer better power gain performance over conventional one. This means proposed cascode structure if acted as a small-signal power amplifier can deliver not only high efficiency, low distortion but better power gain performance when compared to conventional one.

References

[1] W. Shockley: US Patent 2 569 347. (1948).

[2] Y. Takayama and K. Honjo: IEICE Technical Report MW2009-84 (in Japanese). (2009) 61.

[3] Y. Takagi, Y. Takayama, R. Ishikawa and K. Honjo: IEICE Trans. Electron. **E97-C** (2014) 58.