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Characteristics of Submicron Indium-Tin-Oxide Thin-Film Transistors Fabricated by Film Profile Engineering

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Abstract

The first sub-micron (0.4 μm) indium-tin-oxide (ITO) thin film transistor (TFT) fabricated with film profile engineering (FPE) is reported in this work. The devices show very low off-state leakage (<10^{-13} A), extremely high on/off current ratio (>10^{10}), and low subthreshold swing (84 mV/dec). However, severe hysteresis characteristics are also recorded. A model considering the trapping/de-trapping of the induced electrons in the channel is adopted to explain the observation.

1. Introduction

Oxide-based transparent electrodes and thin-film transistors (TFTs) have been widely studied and used in the manufacturing of flat-panel displays, in large part due to the low process temperature in preparing the thin films [1]. Nowadays, thin-film transistors using ZnO or amorphous IGZO have achieved remarkable results, with mobility over 10 cm^2/Vs, good on/off current ratio, and steep subthreshold slope [2]-[4]. However, all these devices are plagued with a mediocre on-current, which is important for driving devices contained in flat-panel displays or high speed circuits [5].

To raise the on-current, indium-tin-oxide (ITO) appears to be a promising channel material. Actually, with its low resistivity and high transparency, ITO has been widely adopted as a transparent electrode in displays and LEDs. Nevertheless, ITO transistors have seldom been reported. *Miyasako et al.* first reported an ITO TFT using ferroelectric-gate in 2005, reaching a high on-current of 2.5 mA [6]. *Dasgupta et al.* fabricated a nanoparticulate ITO transistor in 2008 with an on-current of 0.2 mA but with a mediocre subthreshold slope [7]. In 2009, *Kim et al.* fabricated an ITO FET by solution-based process, reaching a high on/off current ratio of 10^5 but with a mobility of less than 5 cm^2/Vs [8]. In 2010, *Lu et al.* reported a homojunction ITO TFT with one-shadow-mask process. The TFT had a good on/off current ratio of 10^6, with an on-current close to 0.5 mA and good subthreshold slope of 120 mV/dec [9]. The above devices all have significant on-current but suffer from high off current. Also, sub-micron-scale devices have not been reported yet.

In 2013, *Lyu et al.* developed a novel method dubbed "film profile engineering (FPE)" [10] to fabricate ZnO TFTs with sub-micron channel length. In this work, we report on the device performance of ITO TFTs by employing an improved FPE method to fabricate the devices.

2. Experimental Details

A. Device Fabrication

Fig. 1 shows the key process flow used to fabricate the ITO devices. First, SiO_2 and Si_3N_4 were sequentially deposited on a Si wafer to serve as the isolation layers. Then a TiN layer was deposited and patterned to form the bottom metal gate. Next, a SiO_2 sacrificial layer was deposited. After depositing a TiN hard-mask layer, source/drain (S/D) regions were defined with an i-line-based lithographic step. The sacrificial layer was then etched off by selectively wet etching to construct a suspending hard-mask bridge hanging over the bottom gate. The following two deposition steps were the key to realize the FPE concept: (1) SiO_2 with nominal thickness of 50 nm was deposited by plasma-enhanced chemical vapor deposition (PECVD) to serve as the gate dielectric. (2) ITO channel was subsequently deposited by radio-frequency sputtering, under the pressure of 5 mTorr. In the previous FPE study [10], an Al layer was deposited to form S/D contacts in order to improve the device characteristics of ZnO (or a-IGZO) TFTs. Since ITO is a material with sufficiently low resistivity, here we skipped the Al deposition step to simplify the fabrication process. After the SiO_2 passivation layer was deposited, S/D and gate contact holes were opened by inductively-coupled plasma (ICP) etching. From the cross-sectional TEM image (not shown) of an ITO TFT, the sputtered ITO formed an ultra-thin-film of about 15 nm at the central channel.

B. Device Characteristics

Figure 3 shows the transfer curves of a fabricated ITO TFT with channel width/length of 1μm/0.4μm at V_D=0.1 V and 1.1V, respectively. We can clearly see that the off current is less than 10^{-13} A. The on-current is 0.73 mA at V_D=1.1 V and V_G=5 V. The on/off current ratio is over 10^{10}. The threshold voltage defined by G_m method is 1.77V, suggesting an enhancement-mode operation. The field-effect mobility extracted by conventional G_m method [ref?] is anomalously high (> 450 cm^2/V-s) and not reasonable (to be discussed latter). Table I gives a brief summary of the characteristics of the reported ITO TFTs and the results obtained in this study. Our sub-micron TFTs show the best sub-threshold swing and on/ off current ratio among the reported results.

TABLE I
A comparison between reported ITO-based TFTs and this study
(NA: Not available)

Year	Reference	W/L (μm/μm)	SS (mV/dec)	On/off ratio	V_{th}(V)
2005	[6]	120/40	NA	10^4	0
2008	[7]	40/5	230~425	$2x10^3$	*
2009	[8]	500/100	NA	10^5	2
2010	[9]	1000/80	120	10^6	-0.42
This study		**1/0.4**	**84**	**$4.9x10^{10}$**	**1.77**

C. Discussion

A serious counterclockwise hysteresis phenomenon is observed in the I_D-V_G transfer curves (Fig. 3). The hysteresis becomes more severe as the maximum sweeping voltage ($V_{G,max}$) increases. The hysteresis phenomenon can be explained by the trapping/de-trapping model proposed in 2009 by *Lin et al.* [11]. The model suggests that a portion of the induced electrons during the forward V_G sweeping would be trapped by the defects sites located in the grain boundaries of the fully-depleted intrinsic polycrystalline channel. The trapping processes offer an additional (charging) current component in the forward sweeping. This is postulated to be the reason responsible for the anomalously high mobility measured in this study. During the backward sweeping, these trapped electrons stay in the channel until the V_G reaches a sufficiently negative voltage. Higher $V_{G,max}$ would charge more electrons in the channel, thus demanding a more negative gate voltage to release the trapped electrons.

3. Conclusion

ITO TFTs fabricated by a process employing the novel FPE concept are shown to exhibit very high on/off current ratio (>10^{10}), low off current, and steep subthreshold slope. Severe hysteresis phenomenon has been observed and explained by a trapping/de-trapping model. Charging of the traps in the channel is postulated to be responsible for the observation of anomalously high field-effect mobility.

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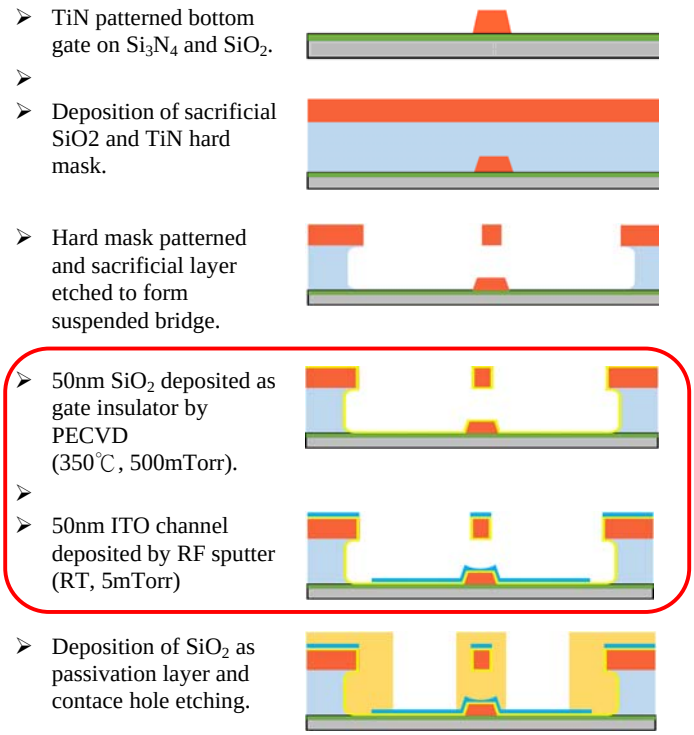

Fig. 1 Key process flow for the fabrication of ITO thin-film transistors. The framed steps denote the FPE steps.

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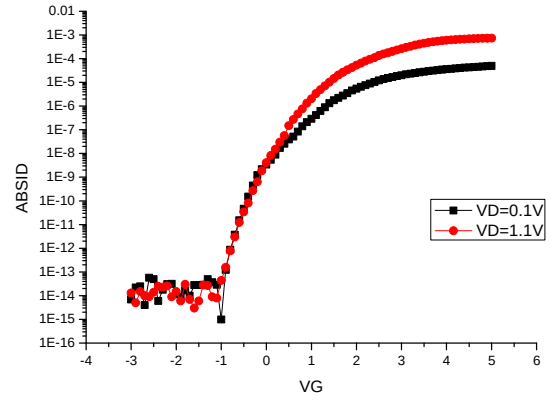

Fig. 2 Transfer curves of an ITO TFT at V_D=0.1V and 1.1V

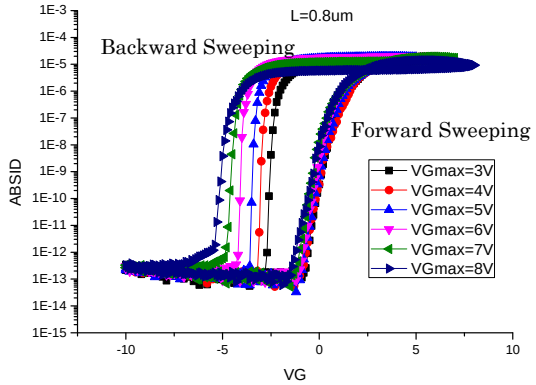

Fig. 3 Transfer curves showing a severe hysteresis effect of the ITO TFT.