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Physical Mechanism of Source and Drain Resistance Reduction in Oxide TFT ~Towards High-Performance Short-Channel InGaZnO TFT~

K. Ota, K. Sakuma, T. Irisawa, C. Tanaka, D. Matsushita and M. Saitoh

Advanced LSI Technology Laboratory, Corporate R&D Center, Toshiba Corporation, 1 Komukai-Toshiba-cho, Saiwai-ku, Kawasaki 212-8582, Japan, Phone: +81-44-549-2192 E-mail: kensuke.ota@toshiba.co.jp

Abstract

We systematically study the mechanism of source and drain parasitic resistance (R_{SD}) reduction in amorphous InGaZnO TFT. Regardless of the S/D processes, R_{SD} reduction is caused by the increase in carrier density. Physical analyses show that the fluctuations of In concentration at the InGaZnO surface are responsible for the enhancement of carrier density. Top-gate InGaZnO TFT fabricated with R_{SD} reduction process shows good short-channel immunity. Short-channel InGaZnO TFT with reduced R_{SD} is promising for high-density back end of line (BEOL) Tr. in Si LSI.

1. Introduction

Recently, InGaZnO TFT for Si-LSI BEOL transistor (Tr.) has been reported [1,2]. For the purpose of high performance and high-density BEOL Tr., top-gate self-aligned short-channel InGaZnO TFT should be realized. However, top-gate self-aligned TFT contains large S/D parasitic resistance between S/D contacts and gate edge as shown in Fig.1. Since S/D diffusion layer cannot be formed by ion implantation in InGaZnO TFT unlike in Si LSI technology, alternative process to reduce R_{SD} is strongly required. There are some reports about R_{SD} reduction in InGaZnO TFT [2-4]. However, the physical mechanisms, such as oxygen vacancies or In segregation at the surface, are still controversial. In this paper, we systematically study the mechanisms of R_{SD} reduction by performing hall measurement and physical analyses such as PL, STEM-EELS and XPS.

2. Sheet Resistance and Hall Mobility of IGZO S/D

We compared several processes such as Ar plasma treatment [2-4], surface N_2 anneal, and surface RIE with CHF_3 for R_{SD} reduction of InGaZnO TFT. It should be noted that InGaZnO film was hardly etched by RIE with CHF_3, thereby only surface region were exposed to the plasma with CHF_3. Sheet resistance of 30nm-thick InGaZnO films deposited by RF sputtering on thermal oxidized Si substrates was measured with 4 probe measurement after each process as shown in Table I. Compared to the sheet resistances of InGaZnO films as deposition or after O_2 anneal, those after Ar plasma treatment, surface N_2 anneal, and surface RIE with CHF_3 were reduced down to the order of 1kΩ/□. We also performed the hall measurement. Fig.2(a) shows the relations between sheet resistance and carrier concentration. Regardless of the processes, sheet resistances are located on a single universal line, indicating that reduction of sheet resistance can be well explained by the increase of carrier concentrations. On the other hand, sheet resistance has no correlation with hall mobility as shown in Fig.2(b). Therefore, R_{SD} can be reduced without sacrifice of mobility. These results suggest that R_{SD} reduction processes are useful as alternatives to ion implantation into S/D diffusion layer in Si technology.

3. Physical Analyses of Treated InGaZnO Surface

In order to clarify the physical mechanisms of R_{SD} reduction, some physical analyses were performed. Fig.3 shows the peak measurement results of the photoluminescence (PL). Peak intensity around 700nm and the half width are plotted against sheet resistance including samples shown in Table I. Peak intensity monotonically decreases while half width increases with decreasing sheet resistance. This suggests that compositional disorder was induced in low resistance film. Fig.4 shows HAADF-STEM images of high resistance and low resistance films. High resistance film shows uniform contrast throughout InGaZnO layer, whereas low resistance film contains different contrast at the surface, indicating that the compositional disorder suggested by PL was induced at the surface.

In order to investigate compositions in InGaZnO layer, STEM-EELS measurement were performed. Figs.5 show depth profiles of each element in high resistance film and low resistance film. Concentration of Ga, Zn, and O are almost the same in high and low resistance films, while In concentration at the surface less than 5nm in low resistance film showed clear reduction, which was not observed in high resistance film. Fig.6 shows the relation between sheet resistance and In concentration at the surface of InGaZnO film measured by XPS. In concentration less than 12% leads to low sheet resistance, irrespective of the S/D processes. It is concluded that R_{SD} reduction was caused by reduction of In concentration in surface region of InGaZnO.

4. InGaZnO TFT with L_g less than 300nm

We fabricated top-gate InGaZnO TFT with T_{ox} of 100nm. In order to reduce R_{SD}, surface RIE with CHF_3 was performed after gate formation. Fig.7 shows TEM image of fabricated InGaZnO TFT. We successfully fabricated short channel TFT with gate length less than 300nm. Fig.8 shows I_d-V_g characteristics. Although the gate oxide was relatively thick, subthreshold slope of 238mV/dec was obtained. Figs.9 and 10 show gate length dependences of threshold voltage and subthreshold slope, respectively. Down to gate length of 400nm, good short channel immunity was observed. Although further improvement of InGaZnO channel quality and S/D contact resistance are required for performance improvement, fabricated InGaZnO TFT showed the potential for short-channel high performance BEOL Tr.

5. Conclusion

Physical origin of S/D parasitic resistance reduction in InGaZnO TFT was investigated. Results from hall measurement, PL, HAADF-STEM, STEM-EELS, and XPS suggest that S/D resistance reduction was caused by the enhancement of carrier density, which was then related to the decrease in In concentration at the InGaZnO surface region (5nm thick). Top-gate InGaZnO TFT showed good short channel immunity down to less than 400nm, indicating potential for high-performance and high-density BEOL Tr. in Si LSI.

Acknowledgment

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References

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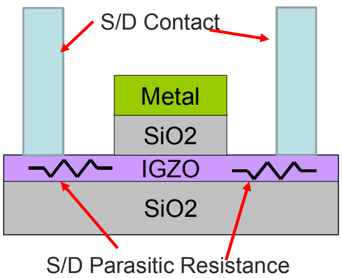

Fig.1 Schematic of InGaZnO TFT. Reduction of S/D parasitic resistance is required for short channel TFT.

No.	Process	Sheet resistance
1	N_2 anneal 320C° 1hour	3.83kΩ/□
2	Ar plasma treatment	2.68kΩ/□
3	surface RIE with CHF_3	1.71kΩ/□
4	surface RIE with CF_4	2.63kΩ/□
5	No.1+ No.2	0.77kΩ/□
6	O_2 anneal 320C° 1hour	>1MΩ/□

Table I. Comparisons between various S/D processes and the sheet resistances.

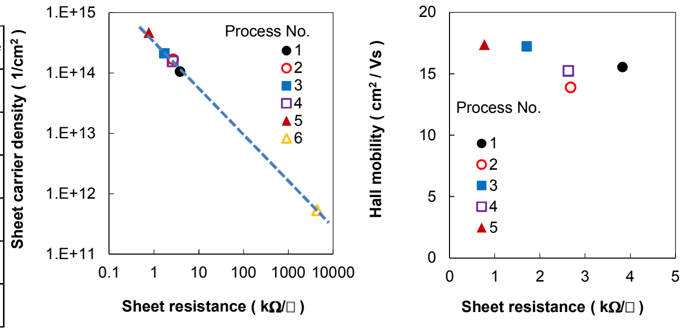

Fig.2 (a) Sheet carrier density and (b) hall mobility are plotted against the sheet resistance. Regardless of the processes, sheet resistances are located on a single line, while sheet resistance has no correlation with hall mobility

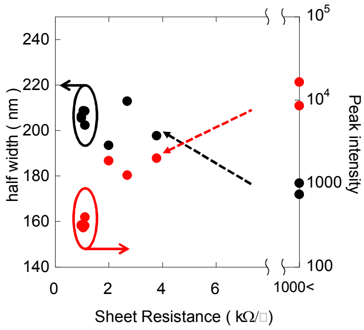

Fig.3 Half width and peak intensity of PL peak around 700nm plotted against sheet resistance.

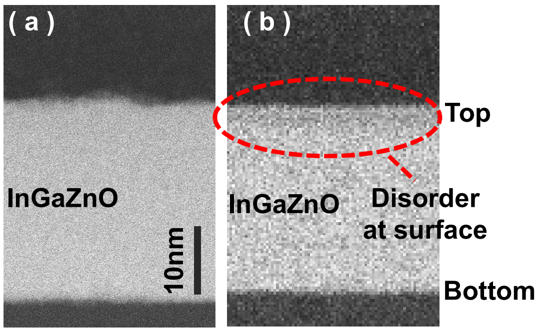

Fig.4 HAADF-STEM images of (a) high resistance and (b) low resistance InGaZnO film. High resistance film shows uniform contrast throughout InGaZnO layer, whereas low resistance film contains different contrast at the surface.

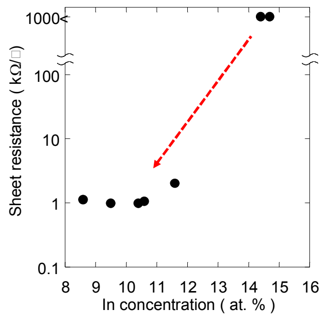

Fig.6 Relation between surface In concentration and sheet resistance measured by XPS. In concentration less than 12% leads to low sheet resistance

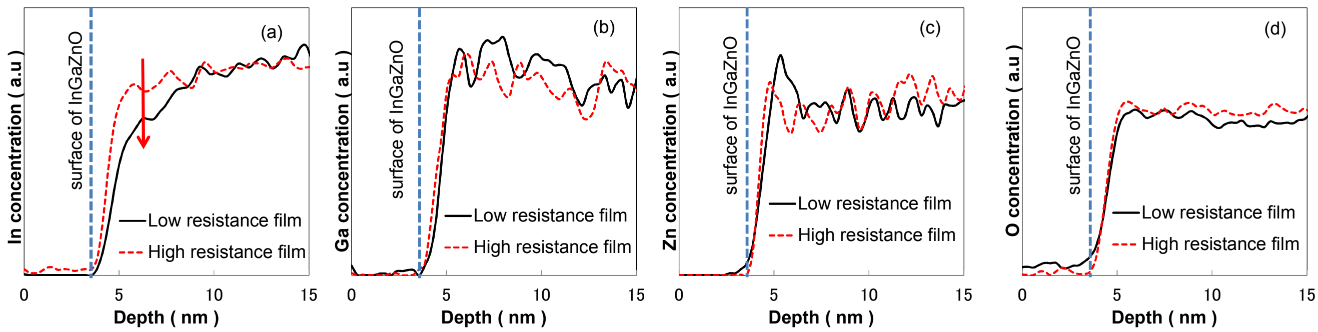

Fig.5 Depth profile of (a) In, (b) Ga, (c) Zn, and (d) O concentrations measured by STEM-EELS. In concentration in low resistance film at the surface is lower than that in high resistance film, while other elements are almost the same.

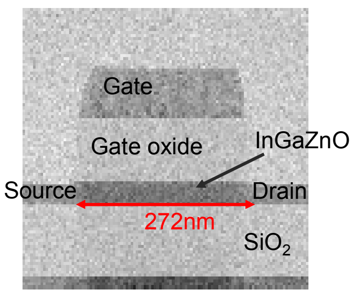

Fig. 7 TEM image of fabricated top gate InGaZnO TFT. short channel TFT with gate length less than 300nm was fabricated.

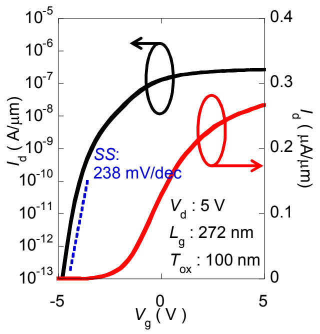

Fig.8 I_d-V_g characteristic of InGaZnO TFT with L_g = 272nm. Subthreshold slope of 238 mV/dec was obtained.

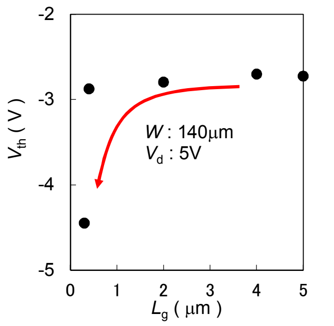

Fig.9 L_g dependence of threshold voltage. Threshold voltage was almost independent of L_g down to 400nm.

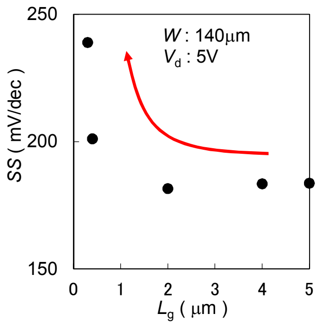

Fig.10 L_g dependence of subthresholdslope. Down to L_g of 400nm, good short channel immunity was observed.