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InGaSb Buried-Channel pMOSFET Fabricated by Using Digital Etch Technique

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Abstract

In this paper, an InGaSb buried-channel pMOSFET has been fabricated by using digital etch technique for active area definition and gate recess etching. The exposed n^+ InAs cap was etched by UV ozone exposure and dilute HCl dip, while the mesa isolation was obtained by using H_2O_2 and HCl:H_2O=1:1 solutions. For a 1 um gate length InGaSb buried-channel pMOSFET, a maximum drain current of about 26.1 mA/mm, a peak transconductance of 9.9 mS/mm, an I_{on}/I_{off} of about 80, and a SS of about 330 mV/decade has been achieved.

1. Introduction

Due to their superior hole mobilities, antimonide-based compound semiconductors such as GaSb and InGaSb have attracted extensive attentions for next generation CMOS integration [1-5]. Hole mobility as high as 1500 $cm^2/V{\cdot}s$ in strained $In_xGa_{1-x}Sb$ channel has been reported [6], which is much higher than silicon and most of other III–V materials. Recent progress in strained InGaSb channel MOSFET makes InGaSb a good competitor in particular for deeply scaled pMOSFET devices. However, future CMOS requires ultra-scaled device architectures such as multigate or nanowire MOSFETs. A method to precisely etch III-Vs heterostructures containing InAs, InGaAs et al. is highly desirable to realize these structures. Recently, record extrinsic transconductance (2.45 mS/um at V_{ds} = 0.5 V) InAs/$In_{0.53}Ga_{0.47}As$ channel MOSFETs by using digital etch technique to remove the exposed n^+ InGaAs cap and upper InGaAs cladding layer [7], and it is reported that digital etch technique is a promising etch technique for ultra-scaled device fabrication [8, 9]. In this paper, an InGaSb buried-channel pMOSFET by using digital etch technique for active area definition and gate recess etching has been fabricated and studied.

2. Experimental

Fig.1 shows the schematic cross-sectional view of the fabricated InGaSb pMOSFET. The starting substrate consists of a 1 um unintentionally doped (UID) $Al_{0.8}Ga_{0.2}Sb$ buffer, a 7.5 nm UID $In_{0.2}Ga_{0.8}Sb$ channel, a 4 nm UID $In_{0.2}Al_{0.8}Sb$ barrier layer, and a 3 nm Si-doped n+ InAs cap sequentially grown on a semi-insulting GaAs (100) substrate by MBE technology. As shown in Fig. 2, after degreased in acetone and IPA, five cycles of digital etch were performed for the active area definition to selectively remove InAs cap, InAlSb barrier, and InGaSb channel, and a part of AlGaSb buffer, H_2O_2 for 1 min was used for oxidation and a HCl:H_2O_2=1:1 solution for 20 sec was used for oxidation removal, then the n^+ InAs cap layer was selectively removed through two cycles of UV ozone exposure and dilute HCl dip, UV ozone exposure for 10 min was used for oxidation of the n^+ InAs cap, a HCl:H_2O=1:10 solution for 30 sec was used for oxidation removal. After an additionally HCl:H_2O_2=1:10 solution for 30 sec, the sample was immediately transferred into the Beneq TFS200 ALD chamber, 10 nm Al_2O_3 was deposited at 300 ^oC as gate dielectric by using TMA and H_2O as precursors. Ni/Au gate electrode was then e-beam evaporated, followed by a lift-off process. After that, Ti/Pt/Au source and drain (S/D) electrode was e-beam evaporated, followed by lift-off process, Al_2O_3 is selectively etched by BOE prior to metal evaporation. Finally, Ti/Au electrode was e-beam evaporated, followed by lift-off process, for device performance characterization. Fig. 3 shows the microphotograph of the fabricated InGaSb buried-channel MOSFET

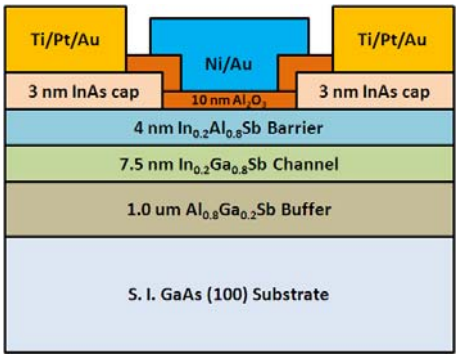

Fig.1 Schematic cross-sectional view of the fabricated MOSFETs

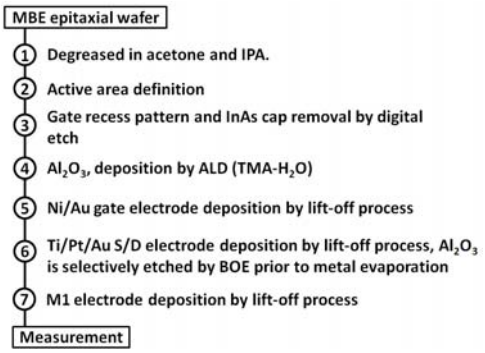

Fig.2 Key process flow for InGaSb pMOSFET

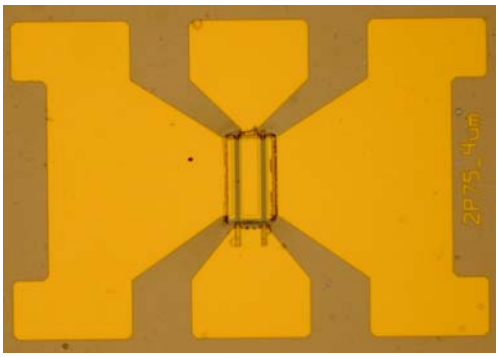

Fig. 3 Microphotograph of the fabricated MOSFET

3. Results and Discussion

The etch rate per cycle of digital etch was measured with Park x-70 atomic force microscope in non-contact mode after multiple cycles of digital etch were performed. For active area definition, after five cycles of digital etch by using H_2O_2 and HCl:H_2O=1:1 solution, the mesa height was about 52 nm, indicating the InAs cap, InAlSb barrier, and InGaSb channel, and a part of AlGaSb buffer were selectively removed. For gate recess pattern and InAs cap removal, after two cycles of digital etch by using UV ozone exposure and dilute HCl dip, about 2.5 nm thick InAs cap layer was selectively removed. The residual InAs cap over the channel region was used to protect InAlSb barrier from been oxidized by air, and the additionally dilute HCl dip was used to etch the residual InAs cap that oxidized by air.

The device performance of the fabricated InGaSb buried channel pMOSFET was characterized by using HP 4155A semiconductor parameter analyzer. Fig. 4 shows the DC output characteristic of a 1 um gate length (L_g) InGaSb pMOSFET with a gate bias (V_{gs}) from 0 to -2 V in steps of -0.5 V, a maximum drain current of about 26.1 mA/mm is obtained at a V_{gs} of -2 V and a drain bias (V_{ds}) of -2 V.

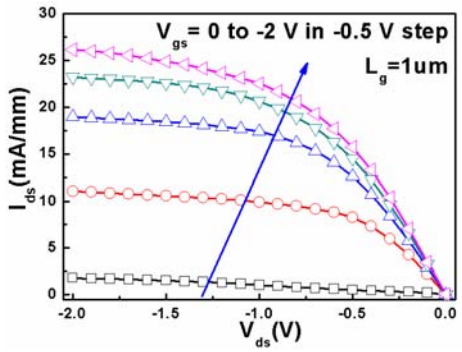

Fig. 4 I_d-V_d characteristics of the fabricated MOSFET.

As shown in Fig. 5, the drain current and extrinsic transconductance vs. gate bias of the same device was measured and calculated with a V_{ds} of -0.5 V, a peak transconductance (G_m) of 9.9 mS/mm is obtained at a V_{gs} of -0.34 V. Fig. 6 exhibits the transfer characteristics of the same device with V_{ds} at -0.5 V and -0.05 V, respectively, the on-current to off-current ratio (I_{on}/I_{off}) is 80, and the sub-threshold swing is 330 mV/decade, the I_{on}/I_{off} and SS are largely limited by the large leakage current of the AlGaSb buffer layer.

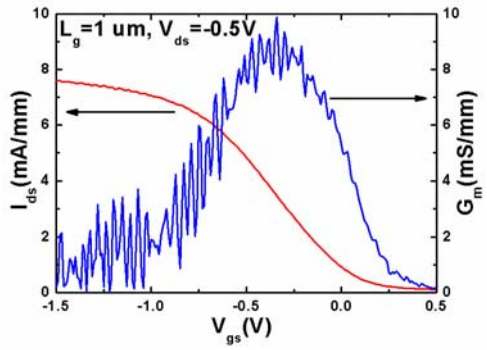

Fig. 5 The drain current and extrinsic transconductance vs. gate bias for the fabricated MOSFET with 1 um gate length at V_{ds} = -0.5 V.

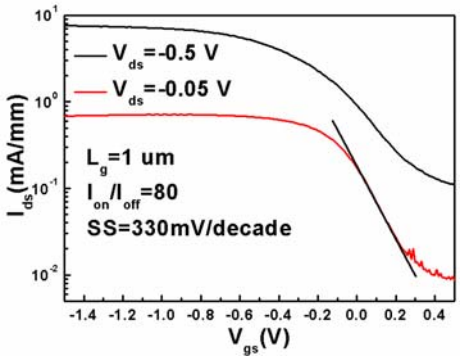

Fig. 6 I_D-V_G characteristic of the fabricated InGaSb channel pMOSFET.

4. Conclusion

In this paper, an InGaSb buried-channel pMOSFET has been fabricated by using digital etch technique for active area definition and gate recess etching. The exposed n^+ InAs cap was etched by UV ozone exposure and dilute HCl dip, while the mesa isolation was obtained by using H_2O_2 and HCl:H_2O=1:1 solutions. For a 1 um gate length InGaSb buried-channel pMOSFET, a maximum drain current of about 26.1 mA/mm, a peak transconductance of 9.9 mS/mm, an I_{on}/I_{off} of about 80, and a SS of about 330 mV/decade has been achieved.

Acknowledgment

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