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Observation of Drain Current Instability on p-GaN Gate AlGaN/GaN HEMTs

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Abstract

In this study, the instability of the drain current on p-GaN gate AlGaN/GaN HEMT is observed. Contrary to the Schottky gate HEMT, I_d-V_d curves of the p-GaN gate devices show dispersion in the saturation region under pulsed condition, which cannot be explained by trapping of electrics in the semiconductor. A model of trapping of holes in the p-GaN layer is proposed for this new observation.

1. Introduction

AlGaN/GaN HEMTs have been identified as one of the most promising devices for high power and high frequency applications. For power applications, enhancement mode operation is needed for fail safe consideration. One of the solutions to achieve E-mode operation in AlGaN/GaN HEMTs is to use a p-GaN gate structure [1]-[3].

In this study, Schottky gate HEMTs for D-mode and p-GaN gate HEMTs for E-mode were fabricated. Drain current instability was observed in the p-GaN gate devices under pulsed conditions while Schottky gate devices were very stable under the same test conditions. This is attributed to the trapping of holes in the p-GaN gate due to non-ohmic metal contact to the p-GaN material. This new finding points out the importance of decent ohmic contact to p-GaN gate for stable device operation which is often overlooked by previous reports.

2. Fabrication and discussion

The AlGaN/GaN epi-layer structures with a total thickness of 5.8 μm were grown on 4-inch silicon wafers with an additional 50 nm p-GaN layer on top of the AlGaN for p-GaN gate devices. The S/D ohmic contacts were formed by depositing Ti/Al/Ti/Au (25/125/45/55 nm), followed by RTA annealing for 30 seconds at 850°C in nitrogen. PECVD oxide (300 nm) and nitride (20 nm) layers were deposited as the passivation layer. A layer of Ni/Au (20/300 nm) was deposited as the Schottky gate metal and as the pad metal. For the p-GaN gate devices, the top p-GaN layer was selectively etched by ICP-RIE with a mixture of BCl3/Ar, and the gate metal was Ni/Au. The device schematics are shown in Fig. 1.

Fig. 2 shows the Id-Vg and transconductance curves of the Schottky gate and the p-GaN gate devices. The Vth for

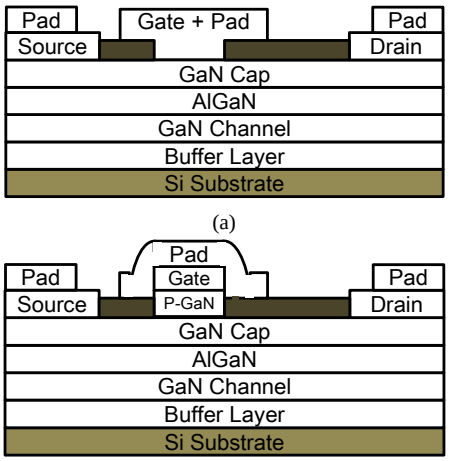

Fig. 1 Schematics of (a) the Schottky gate HEMTs and (b) the p-GaN gate HEMTs

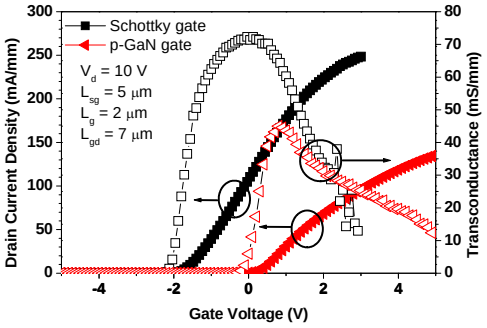

Fig. 2 The Id-Vg and transconductance for the Schottky gate and p-GaN gate devices

the Schottky gate device is -1.5 V and the Vth of the p-GaN gate device is 0.3 V. Fig. 3 shows the measured Id-Vd curves with drain pulses. The pulse width is 5 ms, the period is 50 ms, and the drain base voltage is 0 V. As can be seen in the figure, drain current dispersion is observed in the saturation region for the p-GaN gate device when sweeping from low to high drain voltage, and back. The Schottky gate device, on the other hand, is very stable under the same test conditions. To investigate this phenomenon, pulsed Id-Vg curves were measured as shown in Fig. 4, indicating that holes are trapped in the p-GaN when the base Vg is large enough. The trapping of holes in the floating p-GaN gate as a result of the non-ohmic contact to the

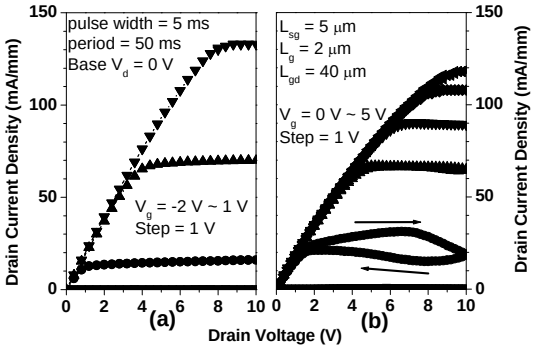

Fig. 3 The Id-Vd curves with drain pulses for (a) the Schottky gate devices and (b) the p-GaN gate devices

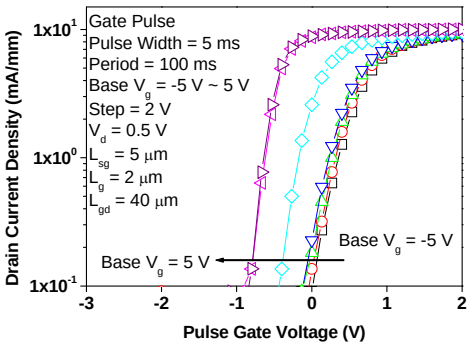

Fig. 4 The Id-Vg curves of the p-GaN gate devices under different gate pulse conditions.

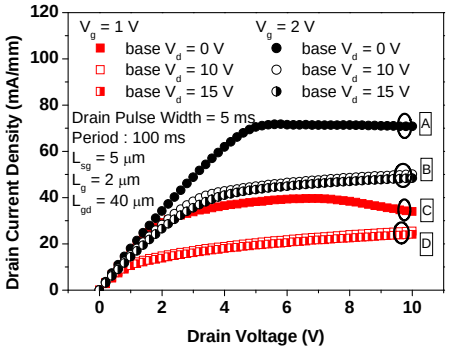

Fig. 5 The pulsed Id-Vd characteristics of the p-GaN gate devices with different drain base voltages.

gate metal causes a negative Vth shift as large as 1 V. Fig. 5 shows the pulsed Id-Vd curves with different drain base voltages. Fig. 6 shows the corresponding energy band diagrams in the gate region under different conditions, assuming a Schottky barrier formed between metal and p-GaN. For condition A, the holes are injected and stored in the p-GaN layer during base period, so the measured drain current during pulse period is enhanced because of negative Vth shift. For conditions B and D, the holes are ejected during base period because the high drain voltage raises the potential underneath the gate. As a result, the drain current decreases because of positive Vth shift. For condition C, The holes are injected into the p-GaN gate during base period, but during the pulse period the drain voltage is also high enough to cause loss of holes. Fig. 7 shows the drain and gate current transients during turn-off at different tem-

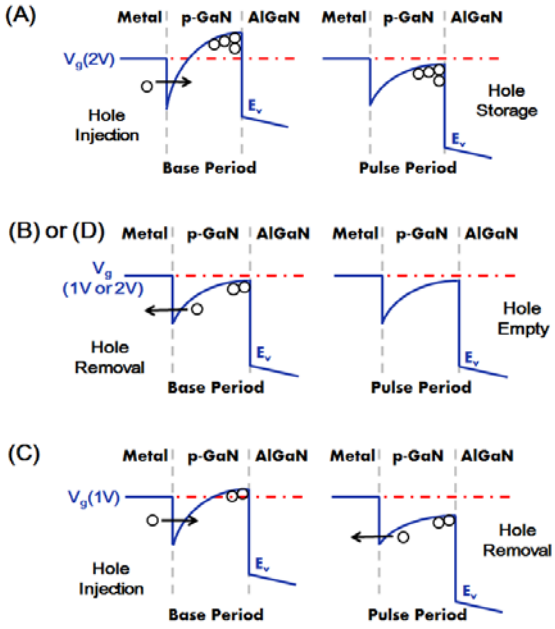

Fig. 6 The valence band diagrams under different pulse conditions (A) to (D) as indicated in Fig. 5.

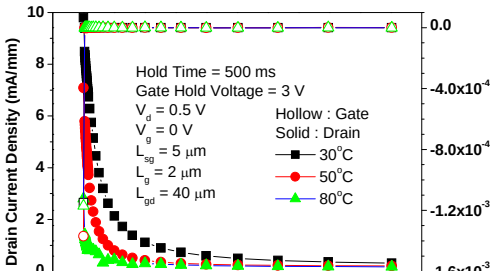

Fig. 7 The drain and gate current transients during turn-off by switching Vg from 3V to 0V at different temperatures.

peratures. The drain current turn-off is much slower than the discharging of the gate, and the turn-off time decreases with temperature which supports our model that holes are ejected over an energy barrier.

3. Conclusions

Schottky gate and p-GaN gate AlGaN/GaN HEMTs were fabricated in this study. Contrary to the Schottky gate devices, the drain current of the p-GaN gate devices showed dispersion with the same pulse measurement, which is attributed to the non-ohmic contact of the gate metal and the p-GaN layer. The trapping and release of holes in the p-GaN layer shifts the threshold voltage and affect the measured drain current under different pulses.

Acknowledgements

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