Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials, Tsukuba, 2014, pp134-135

Study of HfO_2/AlGaN/GaN MOS-HEMT for High Power Application

Wei Cheng Lan[1], Ping Chieh Chin[1], Yueh Chin Lin[2], Jer Shen Maa[3] and Edward Yi Chang[2,4]

[1]Institute of Photonic System, National Chiao-Tung University (NCTU).
1001 Ta Hsueh Road, Hsinchu 30010, Taiwan, R.O.C.
Phone: +886-9-3889-7876 E-mail: function@cycu.org.tw
[2]Institute of Materials Science and Engineering, National Chiao-Tung University (NCTU).
[3]Institute of Lighting and Energy Photonics, National Chiao-Tung University (NCTU).
[4]Institute of Electronics Engineering, National Chiao-Tung University (NCTU).

Abstract

HfO_2/AlGaN/GaN MOS-HEMT with different post deposition annealing (PDA) temperatures is characterized for high power application. The results indicated that AlGaN/GaN MOS-HEMT with HfO_2 as gate insulator have better electrical characteristics, including reduction of gate leakage current and improvement of the drain current degradation under high voltage stress. Furthermore, reliability of HfO_2 MOS-HEMT after PDA 500˚C is more stable compared to other techniques HEMT devices.

1. Introduction

In recent years, GaN-based high-electron-mobility transistors (HEMTs) devices have become one of the most promising power device, due to their excellent electric properties, such as wide bandgap (3.4 eV), high saturation velocity (2.5×10^7 cm/s), large breakdown electrical field (3.3 MV/cm) and great output power density [1].

However, there are several unsolved issues that limit the industry applications of the conventional AlGaN/GaN HEMTs. Gate leakage current is the major problem, which increases power dissipation and decreases the device lifetime for long-term operation [2-3]. Besides, poor long-term reliability of the schottky gate causes serious current degradation.

Recently, effective suppression of gate leakage current and current degradation of AlGaN/GaN HEMT have been demonstrated by inserting a high energy bandgap insulator between gate metal electrode and semiconductor [4]. In this study, we present the electrical performance of AlGaN/GaN MOS-HEMT with HfO_2 as the gate insulator. It shows that the gate leakage current is substantially reduced, and the drain-source current degradation is suppressed as compared the conventional schottky barrier AlGaN/GaN HEMT.

2. Device fabrication and measurement

The samples used in this study are AlGaN/GaN HEMT wafers grown by MOCVD on the silicon substrate. It includes a 1um GaN buffer, a 30nm undoped AlGaN barrier and 1.5nm undoped GaN cap. Both MOS-HEMT and conventional AlGaN/GaN HEMT devices were fabricated for performance comparison. Fabrication process includes mesa isolation, Ohmic contact, and gate information. The mesa isolation was performed using inductively coupled plasma (ICP) etch with Cl_2 gas to define the active region, the etching depth was 200nm. The multilayer metal of Ti/Al/Ni/Au was deposited using E-Gun evaporator and annealed by rapid thermal annealing (RTA) system at 800˚C for 60 sec in N_2 ambient to form Ohmic contact, and the spacing of source-drain was 20um. Finally, Ni/Au gate metal was deposited by E-Gun evaporator, and the gate length used was 2um. Conventional HEMT device (sample S1) was fabricated for comparison. For the MOS-HEMTs, the process steps are the same as conventional HEMT devices except for an insulator thin film (gate dielectric) was deposited between GaN cap and Ni/Au. 7nm HfO_2 was deposited on by molecular beam deposition (MBD) as the gate dielectric. Three samples with various post deposition annealing (PDA) temperatures were prepared: sample 2 (S2), sample 3 (S3) and sample 4 (S4) were individually annealed at 400˚C, 450˚C and 500˚C.

Agilent E5270B power device analyzer was used for DC characterization of the samples and reliability test after long-term high voltage stress. To investigate the long-term current degradation, the devices were stressed for 1 hour at a drain-source voltage (V_{DS}) of 200V with V_{GS}=-5V and the I-V characteristics were measured from off-state to on-state before and after stress.

3. Results and discussions

3.1 DC measurements

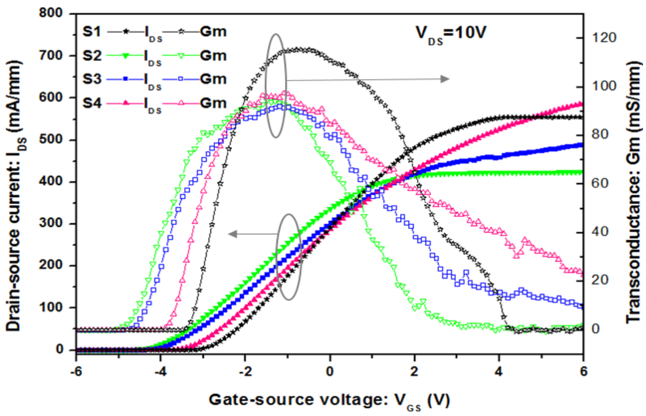

Fig. 1 Comparison of DC characteristics for conventional HEMT and MOS-HEMT: G_m and I_{DS} versus V_{GS} curves.

Figure 1 shows the comparison of the DC characteristics of the four different types of AlGaN/GaN HEMTs. As compared with the conventional HEMT, comparable device

DC characteristics were obtained for the MOS-HEMTs. However, higher maximum drain-source current ($I_{DS,max}$) of 588mA/mm at gate-source voltage of 6V was achieved for the sample 4 as shown in Fig. 1(S1: 555mA/mm, S2: 424mA/mm, S3: 491mA/mm).

3.2 Reliability test

For the high voltage stress test, the AlGaN/GaN HEMTs were stressed at a drain-source voltage (V_{DS}) of 200V with V_{GS} =-5V for 1 hour. The DC characteristics before and after stress for the conventional HEMT and MOS-HEMT are shown in Fig. 2, and the V_{GS} bias was setting from -5 to 3V. It was found that the drain-source current (I_{DS}) decreased for all devices after stressed for 1 hour. However, the current degradation of the conventional HEMT is more serious than the three types of MOS-HEMTs, this is due to the HfO_2 layer effectively suppressed the defect generation and charge injection when the devices were under high voltage stress [1].

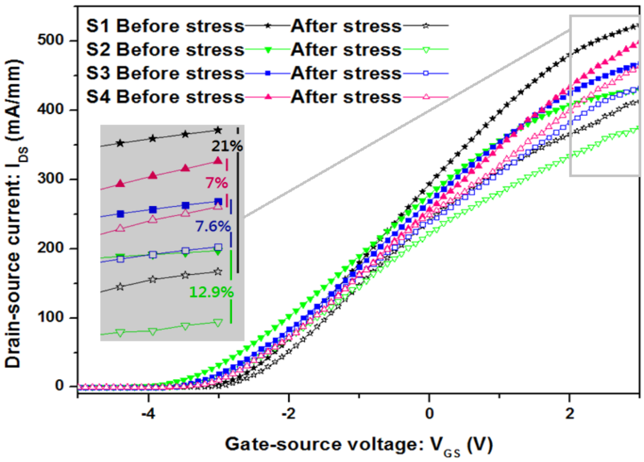

Fig. 2 DC characteristics of the four samples before and after stress.

In addition, Fig. 2 shows that the current degradation of S4 is lower than S2 and S3. This is owing to the interface traps between HfO_2 and AlGaN were favorably reduced by post deposition annealing at 500°C. The effective density of the interface traps D_{it} with different time constants can be estimated using the following expression:

$$D_{it} = \frac{C_{stack} \cdot \Delta V_{fdis}}{q}$$

where C_{stack} is the capacitance of the HfO_2 (7nm) stack and ΔV_{fdis} is the onset voltage dispersion between two frequencies [5]. From figure 3, it is obvious that the D_{it} of S4 is the smallest among the three types of MOS-HEMT studied.

The smaller current degradation indicates that S4 is more stable than the other samples. Furthermore, the threshold voltage of S2, S3 and S4 are -4.7V, -4.5V and -3.7V, respectively.

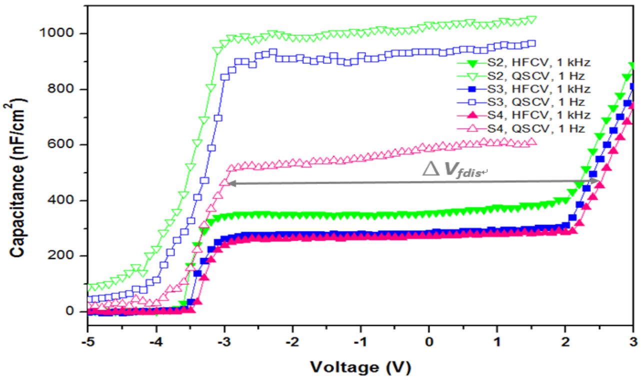

Fig. 3 High-frequency (1 kHz) and quasi-static (1 Hz) C-V curves of the MOS-HEMT with HfO_2 stack as the insulator.

4. Conclusions

An effective insulator technique using 7nm thick HfO_2 film deposited by molecular beam deposition is applied to the fabrication of AlGaN/GaN power MOS-HEMTs. In this study, the MOS-HEMT gate leakage current can be reduced almost 2~4 orders compared to the conventional HEMT in forward bias region. Moreover, MOS-HEMT with HfO_2 as gate insulator can suppress the current degradation under high voltage stress after PDA at 500°C. In summary, MOS-HEMT with HfO_2 gate insulator have demonstrated good potential for high power applications as evidenced by the suppression of gate leakage current and device current degradation.

Acknowledgements

This work was long-term sponsored by the NCTU-UCB I-RiCE program, Ministry of Science and Technology, Taiwan, under Grant No. MOST 103-2911-I-009-302

References

[1] Y. C. Lin, C. H. Chang, F. M. Li, L. H. Hsu, and E. Y. Chang, “Evaluation of TiN/Cu Gate Metal Scheme for AlGaN/GaN HEMT Application,” *Applied Physics Express*, vol. 6, pp. 091003-1– 091003-3, 2013.

[2] Khan M A, Hu X, Tarakji A, et al. AlGaN/GaN metal-oxide-semiconductor heterostructure field-effect transistors on SiC substrates. *Appl Phys Lett,* 2000, 77: 1339-1341.

[3] Mizuno S, Ohno Y, Kishimoto S. Large gate leakage current in AlGaN/GaN high electron mobility transistors. *Jpn J Appl Phys Part 1*, 2002, 41: 5125-5126.

[4] P. D. Ye, B. Yang, K. K. Ng, J. Bude, G. D. Wilk, S. Halder, and J. C. M. Hwang, “GaN metal-oxide-semiconductor high electron mobility transistor with atomic layer deposited Al2O3as gate dielectric,” *Applied Physics Letters*,vol. 86, no. 6, pp.2084-2086, 2005.

[5] Kevin J Chen and Sen Huang, “AlN passivation by plasma-enhanced atomic layer deposition for GaN-based power switches and power amplifiers.” *Semicond. Sci. Technol.* ***28*** *(2013) 074015 (8pp)*