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A self-aligned $Ge/SiO_2/Si_{0.4}Ge_{0.6}$ gate-stacking heterostructure generated in a single fabrication step

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Abstract

We demonstrated a unique approach to generate a self-aligned gate-stacking heterostructure of Ge-quantum dot (QD)/SiO_2/SiGe-shell on Si in a single fabrication step for Ge metal-oxide-semiconductor (MOS) devices, using selective oxidation of a SiGe nano-pillar over a buffer layer of Si_3N_4 on the Si substrate. Intriguingly, a thin 3nm-thick gate oxide of SiO_2 is thermally grown between the Ge QD and SiGe-shell channel with high-quality interfacial properties, which are evidenced by low interface trap density of D_{it} ~ 2—4 × 10^{11} $cm^{-2}eV^{-1}$, low off-state leakage of $I_{off} \cong 10^{-13}$ A/μm, superior switching features of $I_{on}/I_{off} > 10^6$, and subthreshold slope of *S.S.* ~ 305 mV/dec measured on Ge n-MOSFETs. This novel self-aligned gate-stacking heterostructure provides an effective building block for the realization of high-performance Ge gate/SiO_2/SiGe-channel MOSFETs.

1. Introduction

Since the germination of transistors in the late 1940s, germanium (Ge) has been granted as an excellent alternative to their already well-established counterpart Si and a great successor for complementary metal-oxide-semiconductor (CMOS) transistors, because of its superior intrinsic carrier mobility, low dopant-activation temperature, as well as high intrinsic carrier concentration. To date, the key for the realization of Ge CMOS transistors lies in the formation of gate dielectrics on Ge with satisfactory interfacial and electrical properties as well as the growth of Ge on Si heterostructures with sufficiently low defect densities, both of which are extremely challenging [1, 2]. Recently, we have demonstrated a unique approach to generate a Ge-quantum dot (QD)/SiO_2/SiGe-shell heterostructure on the Si substrate in a single fabrication step, by means of the control available through lithographic patterning and selective oxidation of $Si_{1-x}Ge_x$ nano-pillars over buffer layers of Si_3N_4 deposited over Si substrates. In this paper, we further advanced this designer structure to realize high-performance NiGe-gate/SiO_2/SiGe-channel MOS capacitors and transistors, which is evidenced by superior interface properties of D_{it} ~ 2—4 × 10^{11} $cm^{-2}eV^{-1}$, low off-state leakage of $I_{off} \cong 10^{-13}$ A/μm, superior switching features of $I_{on}/I_{off} > 10^6$, and subthreshold slope of *S.S.* ~ 305 mV/dec, thanks to the robust and thermal SiO_2 over Ge.

2. Experimental Works

A tri-layer deposition of 15nm-thick Si_3N_4/20nm-thick poly-$Si_{0.85}Ge_{0.15}$/5nm-thick SiO_2 over the Si substrate was carried out sequentially using low-pressure chemical vapor deposition. Next, using a combination of electron-beam lithography and SF_6/C_4F_8 plasma patterning processes, array of SiGe nano-pillars was fabricated and then subjected to thermal oxidation at 900 °C within an H_2O ambient for the generation of Ge QDs. After the removal of top SiO_2 over the Ge QD, Ni germanidation was performed to generate NiGe gate in a self-organized manner. Then the substrate electrode was made of Al over the backside of the Si substrate. A final forming gas anneal at 400 °C completed the fabrication of NiGe/SiO_2/SiGe MOS diodes. For MOSFETs, additional processes for gate and As-doped source/drain electrodes were implemented.

3. Results and Discussion

Thermal oxidation converts a 230nm-diametered poly-SiGe nano-pillar over a buffer layer of Si_3N_4 into one single spherical, 90nm Ge QD within the Si_3N_4 exactly below each oxidized pillar, as shown in Fig. 1(a). An intriguing finding is that there appears to be a "cup" shaped morphology for the Ge QD/Si substrate interface with an approximately 4—5nm-thick interfacial layer of SiO_2 as well as an approximately 10nm-thick $Si_{0.4}Ge_{0.6}$-shell within the Si substrate, below the interfacial SiO_2 layer. The chemical purity of the Ge QD, thin interfacial layer of SiO_2 and $Si_{0.4}Ge_{0.6}$ shell is verified by elemental line-scanning and mapping examinations of energy dispersive *x*-ray (EDX), as shown in Figs. 1(b)—(c).

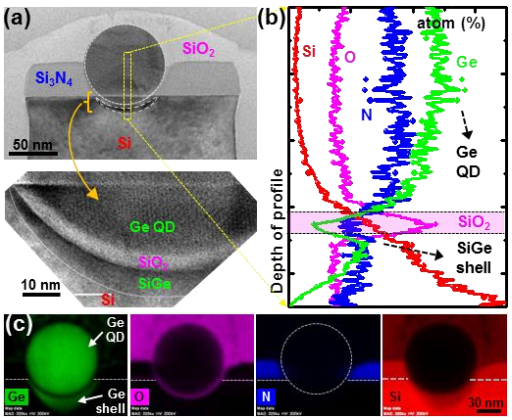

Fig. 1 (a) TEM images as well as EDX elemental (b) line-scanning and (c) mapping examinations of a Ge-QD/SiO_2/SiGe-shell heterostructure on the Si substrate.

Our previous reports have described the mechanism for the self-aligned heterostructure formation of Ge-QD/SiO_2/SiGe-shell on Si [3, 4]. In brief, selective oxidation of a SiGe nano-pillar over buffer Si_3N_4 preferentially converts to the Si within the SiGe into SiO_2 and squeezes separate Ge nuclei inwards to the core of the oxidized pillar. Further oxidation results in the growth of a large spherical Ge QD derived from these Ge nuclei via an Ostwald ripening process as they migrate through underlying buffer Si_3N_4. Attendant to the Ge QD penetration through the buffer Si_3N_4, a thin SiGe shell is generated by the diffusion of Ge atoms into the Si substrate since Ge and Si are totally miscible. A thin interfacial SiO_2 layer between the Ge QD and the SiGe shell is formed by the oxidation of released Si interstitials from the Si-containing layers of Si_3N_4 and Si substrate. This thin but robust and thermodynamically stable SiO_2 is an excellent gate oxide, producing a superior interface between the Ge-QD gate and the SiGe-shell channel.

Figure 2(a) plots capacitance-voltage (*C-V*) characteristics of NiGe/SiO_2/SiGe n- and p-MOS capacitors, respectively. Importantly, neither frequency dispersion nor weak-inversion humps were observable from temperature- and frequency-dependent *C-V* characterisitics. The energy-distribution of extracted interface trap density (D_{it}) exhibits in a typical U-shaped profile with a minimal D_{it} of 2×10^{11} $cm^{-2}eV^{-1}$, as shown in Fig. 2(b).

Figure 3(a) shows that transfer curves of heterostructured Ge-QD gate/SiO_2/SiGe-channel nMOSFETs (L_g/W = 3 μm/ 50 μm) feature high drive current, very low leakage with $I_{on}/I_{off} > 10^6$, and steep subthreshold slope of 305 mV/dec at T = 300K, confirming high crystallinity of the SiGe channel and superior interfacial properties of SiO_2/SiGe. Decreasing temperature not only shifts the threshold voltage positively because of the reduction of intrinsic carrier concentration, but also reduces the subthreshold slope nearly monotonically owing to suppressed thermal fluctuation, as shown in Fig. 3(b). Estimated D_{it} of approximately 10^{11} $cm^{-2}eV^{-1}$ from the subthreshold swing at T = 77 K agrees well with that extracted from *C-V* characteristics. These superior electrical and interfacial properties evince the marvelous nature of self-aligned Ge-QD/SiO_2/SiGe-shell heterostructures that are generated in a single fabrication step, offering great promise for the realization of high-performance Ge MOSFETs.

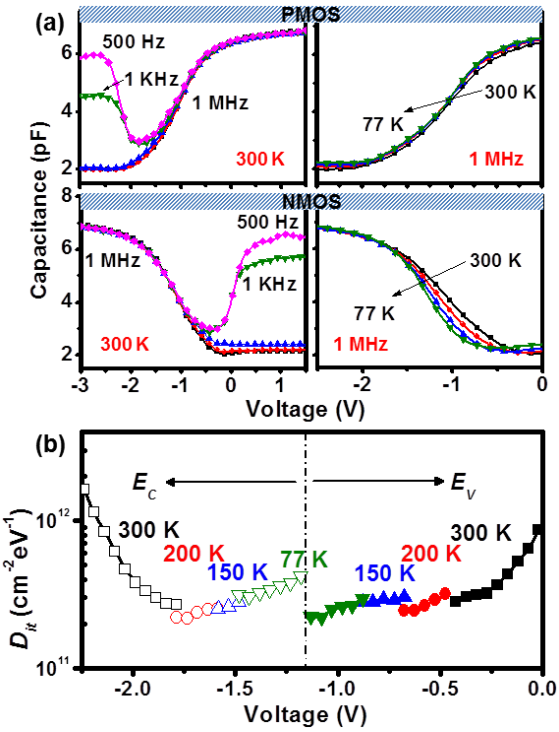

Fig. 2 (a) *C-V* characteristics as a function of frequency and temperature and (b) the extracted D_{it} of a MOS capacitor with NiGe/SiO_2/SiGe heterostructures.

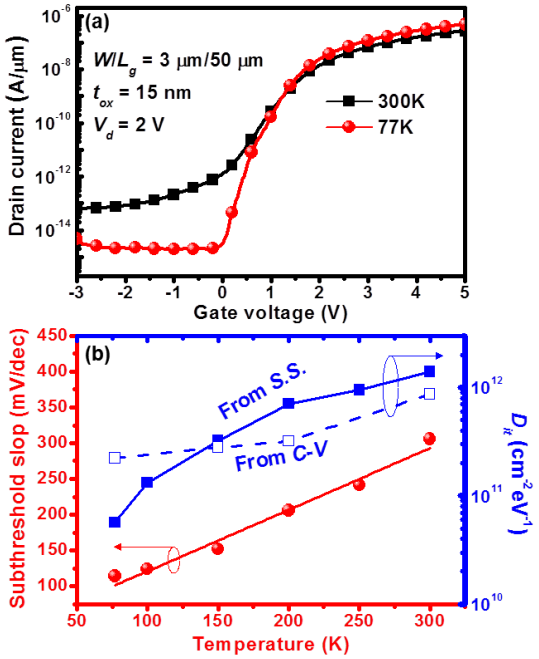

Fig. 3 (a) Transfer characteristics of a MOSFET with an array of Ge-QD/SiO_2/SiGe-shell heterostructures. (b) shows the temperature-dependent subthreshold slop and corresponding D_{it}.

4. Conclusions

In a simple CMOS compatible approach, we demonstrated a novel self-aligned gate stack structure of Ge QD/SiO_2/SiGe shell that has superior interfacial and electrical properties as evidenced by HRTEM, EDX as well as *I-V* and *C-V* characteristics. We envisaged further scientific exploration of this novel heterostructure for the demonstration of advanced Ge QD-based high-speed electronic devices.

Acknowledgements

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