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Investigation and Mitigation of Work-Function Variation for III-V Heterojunction Tunnel FET

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Abstract

This work investigates and compares the impacts of metal-gate work-function variation (WFV) on III-V heterojunction tunnel FET (HTFET), homojunction TFET and FinFET. Due to the broken gap nature, HTFET shows significantly higher susceptibility to WFV near OFF state. To mitigate the variation, device designs are carried out and the source-side underlap is found to effectively reduce the OFF current variation while maintaining satisfactory ON current of the HTFET.

1. Introduction

Tunnel FET (TFET) [1], with its potential in achieving below 2.3kT/q subthreshold swing, has been regarded as a promising device structure for future low-voltage applications. Among various types of TFET, III-V heterojunction TFET (HTFET) [2] has attracted special attention because of its high ON current. With the scaling of device dimensions, random variation emerges as an important reliability concern. Among various variation sources, the work-function variation (WFV) [3] associated with the metal gate has been suggested as the most important variation source for TFET [4]. However, the impact of WFV on HTFET has rarely been known and merits investigation.

In this work, using 3-D atomistic TCAD simulations, we examine the impact of WFV on HTFET. The results will be compared with the III-V homojunction TFET and III-V FinFET, and device design to mitigate WFV is carried out.

2. Simulation Methodology and Device Design

In this work, HTFET composing of GaSb/InAs materials for source/channel is evaluated under the influence of WFV and compared with the homojunction $In_{0.53}Ga_{0.47}As$ TFET and FinFET. In order to describe the characteristics of HTFET and $In_{0.53}Ga_{0.47}As$ TFET, the non-local band-to-band tunneling model [5] that is applicable to account for the arbitrary tunneling barrier with non-uniform electric field is employed with adequate calibrations [6-7] (Fig. 1). Fig. 2 shows the I_{DS}-V_{GS} characteristics of HTFET, $In_{0.53}Ga_{0.47}As$ TFET and $In_{0.53}Ga_{0.47}As$ FinFET at comparable OFF current (I_{off}) and with identical device geometries (Table I). With broken-gap junction, the tunneling width of HTFET drastically decreases to induce significant band-to-band generation rates with increasing V_{GS}, thus enabling steeper subthreshold slope and larger ON current (Fig. 2).

For WFV simulation of the metal gate, the Vonoroi grain pattern [8] for TiN gate is considered with two distinct grain orientations (with 60% and 40% occurring probability and work-function difference of 0.2eV between different orientations as summarized in Table II). For fair comparison, identical grain patterns are utilized for HTFET, $In_{0.53}Ga_{0.47}As$ TFET and $In_{0.53}Ga_{0.47}As$ FinFET with 150 samples for each case.

3. Results and Discussion

Fig. 3 shows the I_{DS}-V_{GS} dispersions for HTFET, $In_{0.53}Ga_{0.47}As$ TFET and FinFET considering WFV at V_{DS} = 0.3 V. As can be seen, HTFET exhibits significantly higher I_{off} variation than other devices. Fig. 4(a) shows the metal-gate grain patterns corresponding to the minimum and maximum I_{off} of HTFET. It is noted that the maximum I_{off} comes from the HTFET with large portion of low-work-function grain patterns near the source/channel junction. On the other hand, metal gate occupied with more high-work-function grain near the junction results in the smaller I_{off}. The impacts of metal-gate grain patterns on band-to-band generation rates and energy bands at V_{GS} = 0V are shown in Fig. 4(b). It can be seen that extremely thin tunneling barrier and higher generation rates are found under the grain pattern with maximum I_{off}. Moreover, due to its broken-gap junction and steeper subthreshold transition, HTFET exhibits drastic degradation in I_{off} for the cases with low-work-function metal grain near the source region, resulting in the significantly higher I_{off} variations than other counterparts. In Fig. 5, the I_{off} and I_{on} variations are compared for HTFET, $In_{0.53}Ga_{0.47}As$ TFET and FinFET. Compared with FinFET, it can be seen that the I_{off} distributions of HTFET and $In_{0.53}Ga_{0.47}As$ TFET (Fig. 5(a)) skew toward higher leakages. This is because at low V_{GS}, the existence of lower work-function metal grain above the critical regions (source/channel junction for HTFET and channel/drain junction for $In_{0.53}Ga_{0.47}As$ TFET) induces significant tunneling current to turn on devices, thus tending to exhibit larger I_{off}. For I_{on} dispersions shown in Fig. 5(b), HTFET shows superior immunity to WFV.

To reduce the inferior I_{off} variation for HTFET (Fig. 3(c)), HTFET designed with various source underlap ($L_{underlap}$) (Fig. 6) is evaluated in the presence of WFV. Fig. 7 compares the I_{on}, average subthreshold swing and I_{off} variations for $In_{0.53}Ga_{0.47}As$ TFET, FinFET and HTFET with different $L_{underlap}$. With the suppression of WFV impact near the source/channel junction, HTFET using source underlap is beneficial to reduce I_{off} variation with increasing $L_{underlap}$ (Fig. 7(c)) at the expense of degraded I_{on} and subthreshold swing (Fig. 7(a) and 7(b)). Specifically, better I_{on} and comparable I_{off} variation to those of $In_{0.53}Ga_{0.47}As$ TFET are observed for HTFET with source $L_{underlap}$ = 10nm. Fig. 8 shows the generation rates and corresponding energy bands for HTFET with and without the underlap region illustrating the smaller influence of WFV on the tunneling junction in the presence of source underlap design.

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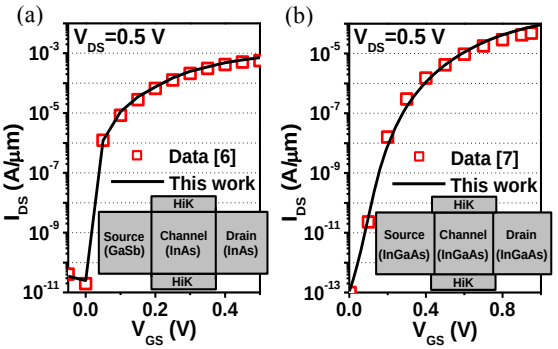

Fig. 1. Calibration of the non-local tunneling model for double-gate (a) GaSb/InAs HTFET [6] and (b) $In_{0.53}Ga_{0.47}As$ TFET [7].

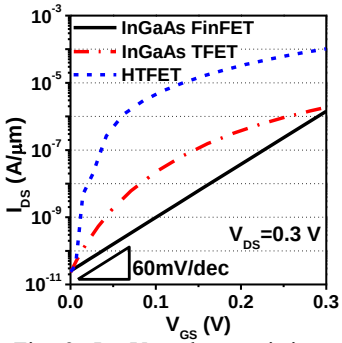

Fig. 2. I_{DS}-V_{GS} characteristics of nominal GaSb/InAs HTFET, $In_{0.53}Ga_{0.47}As$ TFET, and $In_{0.53}Ga_{0.47}As$ FinFET designed with equal I_{off}.

TABLE I. Pertinent Device Parameters

L_g=25nm	W_{fin}=7nm	H_{fin}=20nm	EOT=0.65 nm
Doping (cm^{-3})	**Source**	**Channel**	**Drain**
$In_{0.53}Ga_{0.47}As$ FinFET (n-p-n)	1E19	1E16	1E19
$In_{0.53}Ga_{0.47}As$ TFET (p-i-n)	4.5E19	intrinsic	2E17
HTFET (p-i-n)	4.5E19 (GaSb)	Intrinsic (InAs)	2E17 (InAs)

TABLE II. WFV-related Parameters

Grain Orientation	$In_{0.53}Ga_{0.47}As$ FinFET	$In_{0.53}Ga_{0.47}As$ TFET	HTFET
<200> (60%)	5.01 eV	4.61 eV	4.99 eV
<111> (40%)	4.81 eV	4.41 eV	4.79 eV

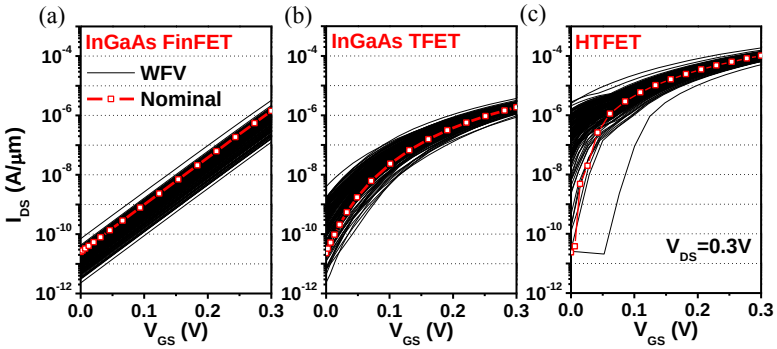

Fig. 3. I_{DS}-V_{GS} dispersions of (a) $In_{0.53}Ga_{0.47}As$ FinFET (b) $In_{0.53}Ga_{0.47}As$ TFET and (c) HTFET considering WFV with 150 samples (average grain size = 5nm).

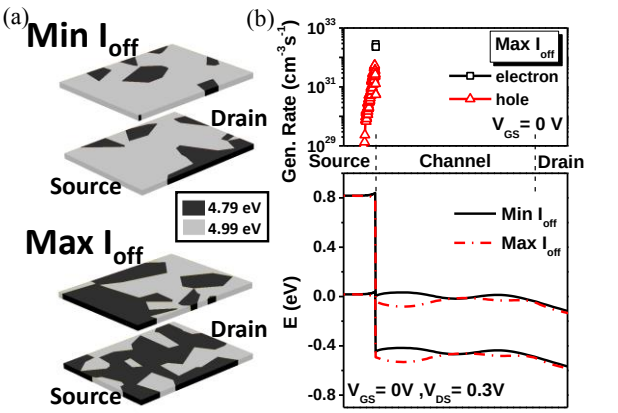

Fig. 4. (a) Metal-gate patterns corresponding to the minimum and maximum I_{off} for HTFET. (b) Electron/hole generation rate and energy band diagram along the channel length direction near the front interface for the cases with maximum and minimum I_{off}. Due to its extremely thin tunneling barrier, electrons/holes are generated close to the junction.

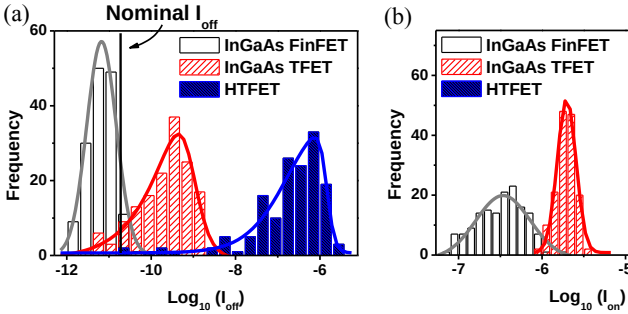

Fig. 5. (a) I_{off} and (b) I_{on} distributions for $In_{0.53}Ga_{0.47}As$ FinFET, $In_{0.53}Ga_{0.47}As$ TFET and GaSb/InAs HTFET considering WFV at V_{DS} = 0.3V.

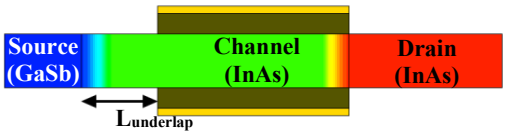

Fig. 6. Schematic of HTFET with source underlap for the mitigation of variability.

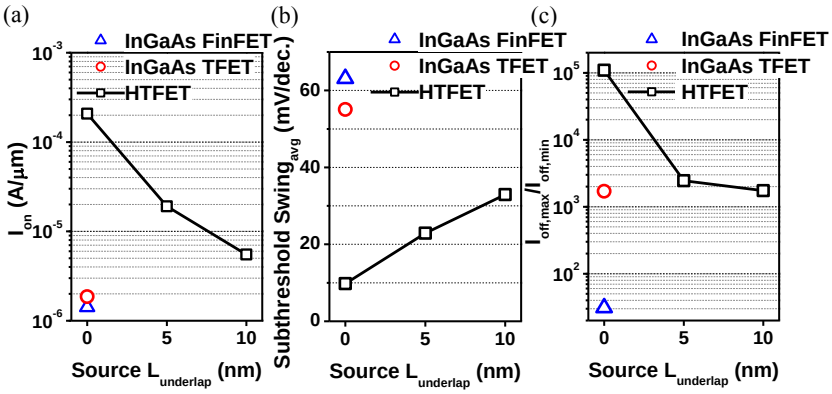

Fig. 7. Comparisons of (a) I_{on} (b) average subthreshold swing (swing between I_{off} and 10^{-6} A/μm), and (c) $I_{off,max}/I_{off,min}$ considering WFV for $In_{0.53}Ga_{0.47}As$ FinFET, $In_{0.53}Ga_{0.47}As$ TFET and HTFET. The HTFETs are designed with various $L_{underlap}$.

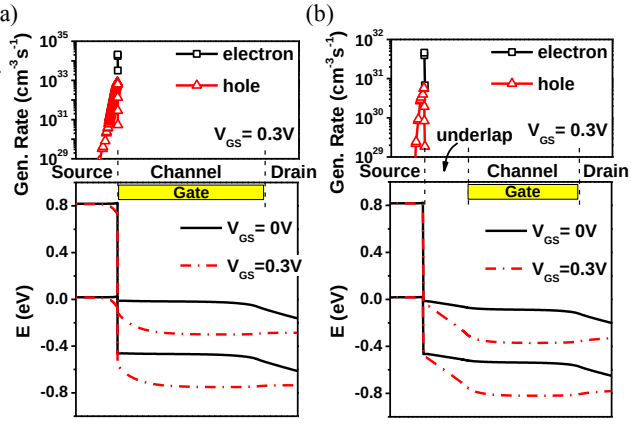

Fig. 8. The electron/hole band-to-band generation rate and energy band diagram for HTFET along the channel length direction near the front interface (a) without and (b) with 10nm source underlap.