

# High Power and High Temperature Operation over 3W/85°C of an InGaN Laser using a Novel Double-heat-flow Packaging Technology

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## Abstract

This paper presents a novel double-heat-flow (DHF) packaging technology of an InGaN laser diode (LD) promising for high power and high temperature operation. The LD chip on a submount is covered by another III-nitride submount with via-hole interconnections, which reduces the thermal resistance with facilitating the assembly in a commercial compact package. A DHF LD operates over 3W at 85°C with maximum output power of as high as 1.9W even at 140°C.

## 1. Introduction

Recently, InGaN LDs have been actively developed for automobile head-lamp and industrial lamp applications because of their distinguished features of long haul illuminations, adaptive distributed beams, and compact optical systems [1, 2]. Although such applications require high light output power under higher temperature ambient than that for consumer electronics, few technological approach has shown over case temperature ( $T_c$ ) of 85°C for InGaN LDs. This paper shows a novel heat dissipation structure which enables output power of more than 3W even under temperature over  $T_c=85^\circ\text{C}$ .

## 2. Concept

In a conventional InGaN LD, only one side of the chip is used as a heat-path as shown in Fig. 1(a). Our concept utilizes another side for the second heat path without losing availability in conventional assembly process.

As shown in Fig. 1 (b), an upper submount is formed on the top surface of an LD for a double-heat-flow (DHF) packaging. Our concept has two novel features. Firstly, the material for DHF packaging is a semi-insulating III-nitride. It has high thermal conductivity and close thermal expansion coefficient to an InGaN LD chip. The latter is advantageous to the metal heat dissipation mount used in conventional bar type LDs [3] in view point of stress. Secondly, the via-hole interconnections and the inner electrode in an upper submount enable the same wire-bonding configuration as that of a single-heat-flow (SHF) LD, which results in the assembly compatibility for commercial compact LD packages.

A DHF packaging technology adds a parallel thermal re-

sistance ( $R_U$ ) to original one ( $R_L$ ) as shown in Fig. 1(c), which reduces a total thermal resistance. As a result, the junction temperature of an InGaN LD decreases, leading to high power / high temperature operations.

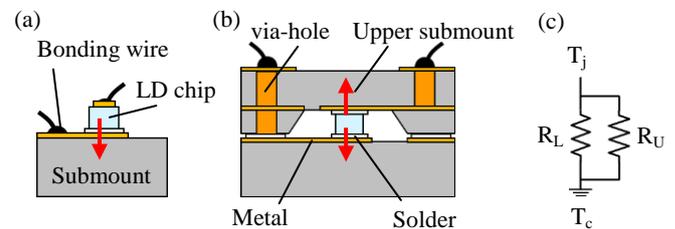


Fig. 1. Schematic drawings of LDs without (a) and with (b) DHF packaging technology. Red arrows indicate heat flows. (c) is a thermal circuit of a DHF LD.  $R_L$  and  $R_U$  are the thermal resistance of lower and upper heat paths respectively.

## 3. Design

To clarify the performance of a DHF LD, thermal saturation power  $P_{\max}$  is calculated as a function of thermal resistance of an upper submount. This calculation assumes that the  $P_{\max}$  is limited only by the thermal saturation, since watt-class LDs use wide stripe structures and suffer from little catastrophic optical damage. Empirically,  $P_{\max}$  and the wall plug efficiency  $\eta_{\max}$  at  $P_{\max}$  are modeled as;

$$P_{\max} = P_0 \cdot \{1 - \alpha \cdot \exp(-E_1/kT_j)\}, \quad (1)$$

$$\eta_{\max} = \eta_0 \cdot \{1 - \beta \cdot \exp(-E_2/kT_j)\}, \quad (2)$$

where junction temperature  $T_j$  is expressed as

$$T_j = T_c + R_{th} \cdot (1/\eta_{\max} - 1) \cdot P_{\max}. \quad (3)$$

$R_{th}$  equals total thermal resistance and equals  $1/(1/R_U+1/R_L)$ .  $k$  is a Boltzmann constant.  $P_0$ ,  $\alpha$ ,  $E_1$ ,  $\eta_0$ ,  $\beta$ , and  $E_2$  are fitting parameters, which are obtained experimentally using conventional SHF LDs in continuous wave (CW) operations. Based on the above, Eqs. (1) – (3) are calculated self-consistently as shown in Fig. 2. It shows a DHF packaging technology dramatically increases the saturation power of an InGaN LD. This increase is distinguished especially under high temperature, which expects watt-class output power operation even at  $T_c=140^\circ\text{C}$ .

When AlN is applied for an upper substrate material with the same physical dimensions as those in the following experiment,  $R_U$  is calculated as 12.4 K/W. For this  $R_U$ , Fig. 2 indicates that the saturation power of a DHF LD will be approximately 4 W at  $T_c=85^\circ\text{C}$ . Figure 3 shows the calculated thermal distribution in LD chip with and without a DHF packaging technology. It indicates clearly that the upper submount works as the second heat path. By using a DHF packaging technology, estimated  $R_{th}$  decreases from 10.5 K/W to 6.5 K/W, which dedicated to lowering a junction temperature.

#### 4. Experimental

InGaN LD layers were grown on an n-type GaN substrate using metal organic chemical vapor deposition. The emission wavelength is around 405nm. The cavity length is 1150 $\mu\text{m}$ . The upper submount consists of 2-layer AlN plates, 300 $\mu\text{m}$ -dia. via-holes filled with W, and Au-Sn spacer/electrode. SiC is used for the lower submount. In the assembly, an InGaN LD was soldered to the lower submount in junction up configuration, followed by upper submount soldering using Au-Sn bump pellets. Both upper and lower submounts have the same length and width, which are 1330 $\mu\text{m}$  and 1600 $\mu\text{m}$ , respectively. The LD was assembled in a commercial compact TO-9 package.

Figure 4 shows the SEM cross section view of a DHF LD, which shows rigid contact between a LD chip and upper/lower submounts. Such a contact is preferable for mechanical robustness and thermal resistance reduction.

The thermography image of a DHF LD is shown in Fig. 5. The heat loss of the LD is about 2W. The heat flow through the upper submount is clearly observed. Since temperature increase of the LD is 12 $^\circ\text{C}$ , the total thermal resistance of the DHF LD is measured as 6K/W.

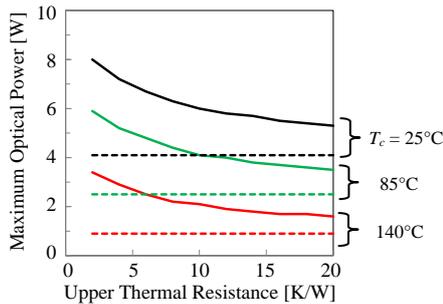


Fig. 2. Calculated  $P_{max}$  of a LD with a DHF packaging technology (solid line) and  $P_{max}$  of a SHF LD (dotted line).  $R_U$  is 12.4K/W.

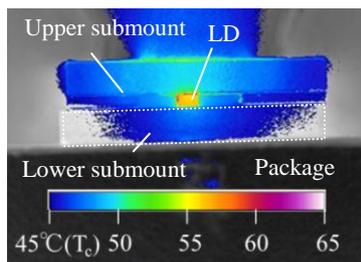


Fig. 5. Thermography image of front view of a DHF LD.

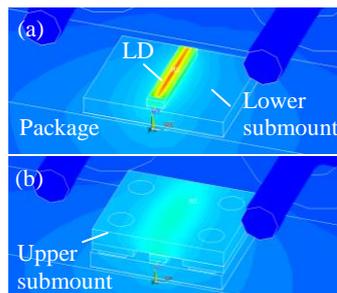


Fig. 3. Calculated thermal distribution in LD chip without (a) and with (b) a DHF packaging technology.

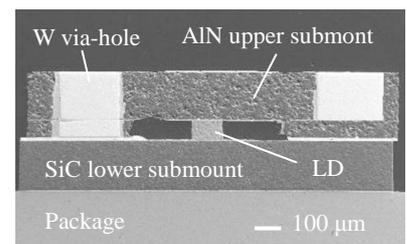


Fig. 4. SEM image of cross section view of a DHF LD.

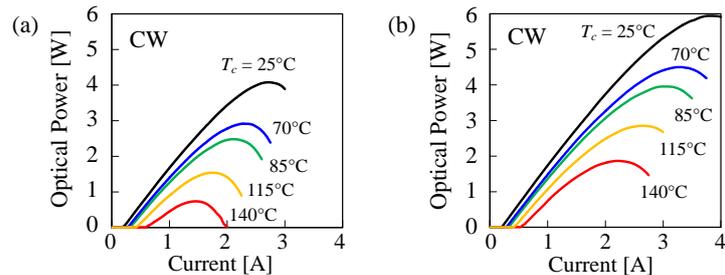


Fig. 6. CW current-optical power characteristics of LDs without (a) and with (b) a DHF packaging technology.

Figure 6 shows CW current-optical power characteristics of InGaN LDs with and without a DHF packaging technology under various temperatures. At  $T_c=25, 85,$  and  $140^\circ\text{C}$ , although  $P_{max}$ s of the LD without a DHF packaging technology are 4.1, 2.5, and 0.7 W, these with DHF packaging technology increase up to 5.9, 4.0, and 1.9W, respectively. The  $P_{max}$ s above are almost same as the expected ones as shown in Fig. 2.  $P_{max}$  of the DHF LD at  $140^\circ\text{C}$  is 2.7 times higher than that without one.

#### 5. Conclusions

We have developed the novel double-heat-flow packaging technology for realizing high power and high temperature operation of InGaN LDs. The upper submount, which consists of a III-nitride material with via-hole interconnections, increases maximum output power and facilitates assembly process in commercial TO-9 package. Maximum CW output power of the DHF LD is more than 3W at  $T_c=85^\circ\text{C}$  and as high as 1.9W even at  $T_c=140^\circ\text{C}$ .

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#### References

- [1] K. Takahashi *et al.*, Sharp Technical Journal, **104** (2012) 23 [in Japanese].
- [2] C. Altingöz., Proc. SPIE, High-Power Diode laser Technology and Applications XII, **8965** (2012) 896518.
- [3] P. Loosen: in *High-Power Diode Lasers*, ed (Springer, Bellin, 2000) p.289.