

Ultra-Compact 100Gb/s Coherent Receiver Monolithically Integrated on Silicon

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Abstract

We present an ultra-compact coherent receiver monolithically integrated on Silicon. It integrates all components in an area of only $1.3 \times 1.4 \text{ mm}^2$, which is about half the size of the smallest reported. Receiving of 100Gb/s PDM-QPSK signal is also successfully demonstrated.

1. Introduction

With the high-pace development of optical transmission systems, their performances such as high bandwidth, high spectral efficiency, and low cost are in great need [1]. A promising scheme is the optical coherent transmission, and it has become a key technology for the high capacity, long-haul communications with channel data rates at 100Gb/s and beyond [2]. In a coherent detection system, larger bandwidth is usually obtained by using the polarization-division-multiplexed quadrature phase-shift keying (PDM-QPSK) or even higher-level modulation formats. Coherent detection can convert the amplitude, phase, and polarization of an optical signal into the electrical domain, thus enabling high sensitivity, high spectral efficiency. However, traditional coherent receivers are usually built up by discrete element components such as polarization beam splitters, 90° hybrids and photodetectors, which increase the system size, power consumption, and heat dissipation. Thus compact, low cost and energy-efficient coherent receivers are in stringent need.

Silicon (Si) photonic integrated circuits (PICs) are attracting considerable attention because of its compatibility with complementary metal oxide semiconductors (CMOS) technology, small foot print, high yield and thus low cost. In a Si PIC, the element components are interconnected on a single Si chip so that it becomes much easier to ensure the optical path-length to be well matched and balanced. Recently, there are many reports of monolithically integrated coherent receiver on Si PICs [3-5], which demonstrate their high potential in achieving high performance coherent receivers.

In this paper, an ultra-compact polarization and phase diversity coherent receiver is demonstrated by using the Si PICs. The foot-print of the coherent receiver is about half as large as the best reported results ($3 \text{ mm} \times 1.3 \text{ mm}$) [5]. For the reception of high speed PDM-QPSK signal, it only requires 17dB optical signal-to-noise ratio (OSNR) at 10^{-3} bit-error rate (BER).

2. Design of the Silicon PIC

The schematic of the coherent receiver is shown in Fig.

1(a). The coherent receiver PIC includes one 2D grating coupler, one 1D grating coupler, one 1×2 multimode interference (MMI) splitter, two 90° hybrids, and four pairs balanced Germanium (Ge) photodetectors (PDs). In each pair, the PDs are connected in series. Every two pairs in each side of the PIC share the same direct current (DC) bias connections. On-chip capacitors are also designed to have good connection with the ground pads for high speed signals. More specific designs and performances of the element components are explained in Ref. [6].

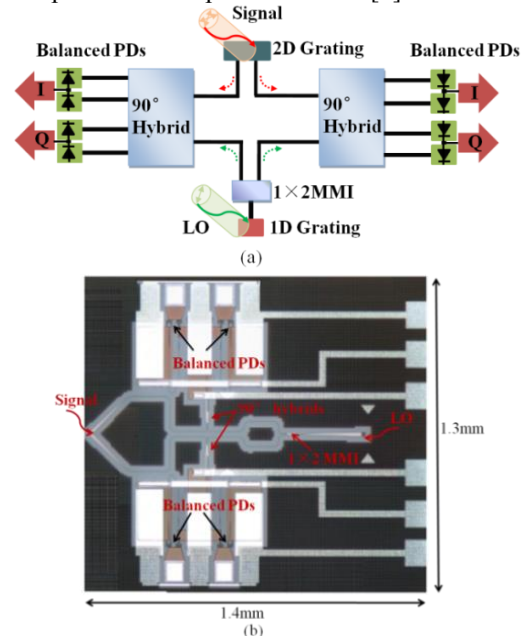


Fig. 1 (a) Schematic of the coherent receiver. (b) The optical microscope image of the fabricated coherent receiver PIC.

The working principle of the coherent receiver is as follows. Via the 2D grating, the optical signal in the optical fiber can be coupled into the PIC. Once coupled in, the signal light are divided into two TE polarizations light. Meanwhile, the TE polarization local oscillator (LO) light is coupled into the chip through the 1D grating coupler. Then it is divided into two by the 1×2 MMI splitter. The divided signal and LO light propagate in two different directions, and proceed to the corresponding 90° hybrids [7]. The outputs of the 90° hybrids are detected by the balanced PDs. The balance detection in both sides of the receiver can generate the in-phase and quadrature components accordingly. By subsequent off-line digital signal processing, the amplitude and phase information of the received signal can be achieved.

The coherent receiver PICs were fabricated on a Silicon

on insulator (SOI) wafer with top Si thickness of 220nm. The Si waveguides in the receiver PICs are ridge type with the slab thickness is 90nm. The fabrication processes are performed by the standard foundry technology for Si PICs, mainly including passive Si waveguide patterning and formation, Ge epitaxy on Si substrate, ion implantations and subsequent annealing for ohmic contacts, metallization and final bond pad opening. The optical microscope image of the fabricated coherent receiver PIC is shown in Fig. 1(b).

3. Experimental Results

For the 1D grating coupler, we have achieved a coupling efficiency of 43%, and the 3dB bandwidth of the optical spectrum is about 48nm [6]. As to the 2D grating coupler, the coupling efficiency is 20%, the extinction ratio is larger than 25dB, and the 3dB bandwidth is measured to be 50nm, as shown in Fig. 2(a) and Fig. 2(b). Our 90° hybrids are designed for TE mode without any additional phase shifter or waveguide crossing for the coherent receiving system [7]. Each 90° hybrid consists of cascaded wedge-shaped 2×4MMI coupler and a 2×2MMI coupler. The extinction ratio is larger than 20dB and the phase deviation is within the range of 5° over C-band wavelength range, as shown in Fig. 2(c) and Fig. 2(d). Moreover, the total length of our wedge-shaped 2×4 MMI coupler is only 107μm, which is the smallest size among the reported 90° hybrids based on MMI couplers. The dimension of the Ge PD is 1.6μm×10μm. The dark current is 0.56μA at -1V [6]. And the responsivities are 0.63A/W and 0.94A/W at -1 and -2V bias respectively. The 3dB bandwidth is larger than 20 GHz at -3.5V bias, as shown in Fig. 2(e) and Fig. 2(f).

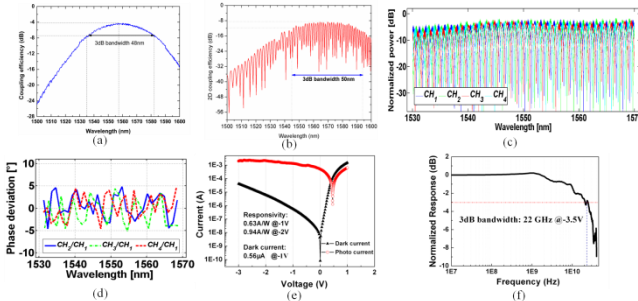


Fig. 2 Basic performances of the element components.

In order to check the viability of the coherent receiver in 100Gb/s optical transmission systems, we initially undertook the following experiments. Prior to the further package with transimpedance amplifiers (TIAs), both two parts of the coherent receiver PICs are measured separately. For the upper part in Fig. 1(b) measurement, we launched a TE polarization 50Gb/s QPSK signal of 9.98dBm at 1547.715nm wavelength into the 2D grating port, and a CW laser of 15.5dBm into the 1D grating LO port. The 50Gb/s QPSK signal was generated by the commercial high speed transmitter module. The outputs of the balanced PDs were probed by the high speed 50Ω terminated Ground-Signal-Ground-Signal-Ground (GSGSG) probes and then connected to the 80GS/s real-time oscilloscope. Then the sampled data were processed off-line using the standard digital signal processing algorithms. By off-line

processing, we obtained good signal constellations as shown in Fig. 3(a). By comparing millions of received data with the original launched ones, we calculated the bit error rate (BER) versus different optical signal-to-noise ratios (OSNRs). As can be seen from Fig. 3(c), it only requires about 17dB OSNR at 10^{-3} bit-error rate (BER). Then we changed the 50Gb/s QPSK signal into TM polarization and probed the outputs of the down side of the receiver as shown in Fig. 1(b). Following the same off-line processing, we got similar constellations as shown in Fig. 3(b). Both parts of the coherent receiver have demonstrated satisfactory performance at 50Gb/s. By polarization multiplex, we can achieve the 100Gb/s polarization and phase diversity coherent detection. After packaging with TIA, our coherent receiver is surely being able to well receive the 100Gb/s PDM-QPSK signals. Further package design and measurement work are underway.

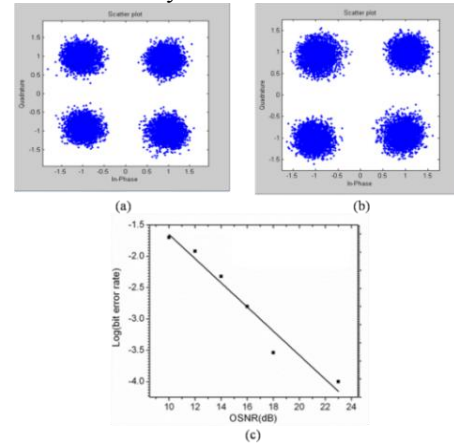


Fig. 3 (a) Signal constellations for TE polarization. (b) Signal constellations for TM polarization. (c) Calculated BER versus OSNR for 50Gb/s QPSK signal.

4. Conclusions

We demonstrate a monolithically integrated coherent receiver on Si, with an ultra small footprint of $1.3 \times 1.4 \text{ mm}^2$. The coherent receiver can successfully detect the 100Gb/s PDM-QPSK signal. This high-level integration makes Si PICs good solutions to provide low cost transceivers for future optical communication systems with channel data rates at 100Gb/s and beyond.

Acknowledgments

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