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Suppression of void generation in direct wafer bonding for Si high-k MOS optical modulators using Al_2O_3/HfO_2 bonding interface

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Abstract

We have investigated the reduction of void generation on the bonded wafers fabricated by thin-EOT direct wafer bonding (DWB) method for MOS optical modulators. Although the voids cannot be completely removed from the bonded wafer using Al_2O_3, the voids are successfully eliminated from the bonded wafer using Al_2O_3/HfO_2 when annealing temperature is up to 700ºC.

1. Introduction

A metal-oxide-semiconductor (MOS) optical modulator is one of candidates for achieving ultra-high modulation efficiency in Si photonics. There are several reports about the MOS optical modulators [1-3], in which a poly-Si/SiO_2/Si gate stack is commonly used to form the MOS structure. However, there are two technology issues to realize high-performance MOS optical modulators: one is the crystal quality of poly-Si gate and the other is lack of equivalent oxide thickness (EOT) scalability. The large grain size in poly-Si is preferable for achieving low resistivity, while the increase in optical scattering loss is unavoidable. Thus, there is a tradeoff between low resistivity and low optical loss in poly-Si. Meanwhile, it is difficult to scale the thickness of SiO_2 down to less than 3 nm due to an increase in gate leakage through quantum tunneling. To achieve the low-$V_\pi L$ MOS optical modulators, we have investigated the effect of EOT scaling by using high-k dielectric [4]. However, the formation of poly-Si/high-k gate stack is more difficult than that of poly-Si/SiO_2 gate stack due to its low thermal budget. Thus, to overcome these issues, we propose to use a thin-EOT direct wafer bonding (DWB) for Si high-k MOS optical modulators. Fig. 1 shows a schematic fabrication procedure of a thin-EOT MOS optical modulator by DWB. Using this technique, we can achieve the superior quality of crystallized Si gate with thin EOT. However, the generation of voids at bonded interfaces during high-temperature annealing is one of the major obstacles for device fabrication. Thus, in this paper, we have discussed how to reduce the void generation of thin-EOT DWB. By introducing Al_2O_3/HfO_2 interfacial layer for bonding, we have successfully suppressed the void generation by a few orders of magnitude.

2. Experimental

Fig. 2 shows the process flow of the direct wafer bonding using Si-on-insulator (SOI). After pre-cleaning by HF, Al_2O_3/HfO_2 is deposited on each substrate by atomic layer deposition (ALD) at 300ºC. Then, a post deposition annealing (PDA) is carried out at 400ºC or 700ºC for 20 min in vacuum. After cleaning the surface of the substrates by a mega-sonic cleaner, the two substrates are manually bonded in air. Then, the bonded substrate is pressed and annealed under 3000 N weight at 350ºC for 1 h. After bonding, top Si is mechanically polished with a thickness down to 100 μm and the remained Si is etched by TMAH. Then, the top SiO_2 is etched by BHF. The bonded substrates are annealed to confirm void generation on the substrates.

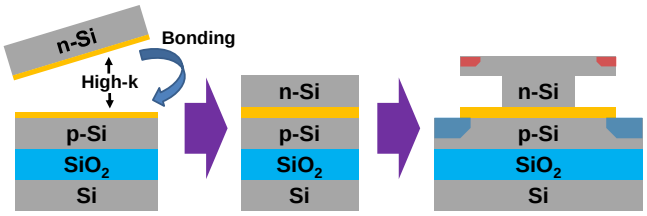

Fig. 1. Schematic process flow of a thin-EOT MOS optical modulator using direct wafer bonding technique.

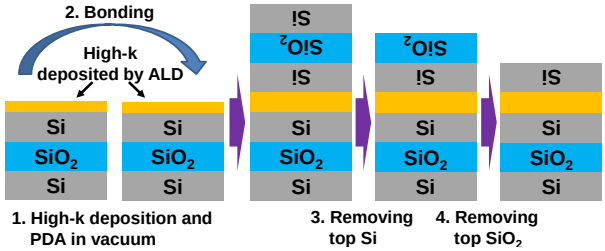

Fig. 2. Process flow of direct wafer bonding for high-k MOS modulator using high-k dielectric.

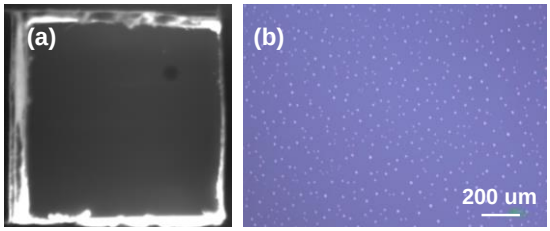

Fig. 3. (a) IR image of the bonded wafer using Al_2O_3. (b) Microscopic image after removing top Si and SiO_2.

Fig. 3(a) shows the IR image of the bonded wafers using 4.5-nm-thick Al_2O_3 gate stack. This image is taken after pressing at 350ºC for 1 h. As shown in Fig. 3(a), there are few de-bonded regions on the bonded wafer; thus the bonding is successfully carried out. Fig. 3(b) shows the microscopic image of the bonded wafers after etching top Si and SiO_2. As shown in Fig. 3(b), there are many micro-voids which cannot be detected by the IR image.

We consider that these micro-voids were caused by the degassing of water from the Al_2O_3 layer. To reduce these micro-voids, we have optimized the purge time of water for the Al_2O_3 recipe of ALD. The purge time is changed from 1 s to 27 s. Fig. 4 shows the relationship between the density of voids and the purge time of water. As the purge time increases, the micro-voids are significantly reduced by an order of magnitude.

To confirm the thermal stability of the bonded wafers using long-purge-time Al_2O_3, we have also investigated number of voids generated after 1-min annealing by rapid thermal annealing (RTA). The annealing temperature ranges from 400ºC to 600ºC. Fig. 4 shows the relationship between the RTA temperature and the density of the voids. The void density is significantly increased when the annealing temperature is over 500ºC; thus the high-temperature process is unacceptable for the bonded wafer using the Al_2O_3 gate stack.

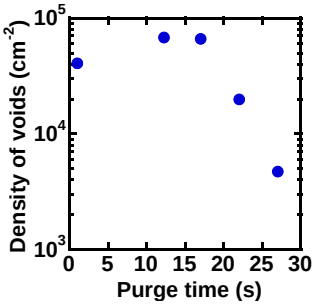

Fig. 4. Relationship between the density of micro-voids and the purge time of water in ALD process for Al_2O_3.

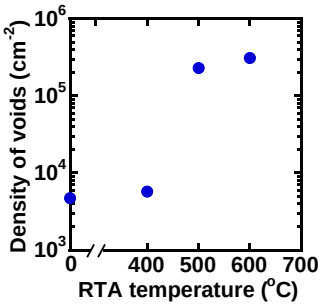

Fig. 5. Relationship between the density of micro-voids on the bonded wafer using Al_2O_3 and the annealing temperature of RTA for 1 min.

To obtain bonded wafers with high thermal stability, we introduce HfO_2 for the bonding interface. Fig. 6(a) shows the IR image of bonded wafers using 1.5-nm Al_2O_3/2.0-nm HfO_2/0.5-nm Al_2O_3. The purge time of Al_2O_3 is 1 s. Since the bonded wafer using only HfO_2 is detached after etching the top Si substrate by TMAH, we still insert Al_2O_3 as an adhesive layer for bonding. Fig. 6(b) is a microscopic image of the bonded wafer after removing the top Si substrate. It is found that micro-voids are not observed even when the purge time of Al_2O_3 is as short as 1s. Thus, we can conclude that HfO_2 is effective to reduce the micro-void generation during the bonding process.

To confirm the thermal stability of $Al_2O_3/HfO_2/Al_2O_3$ DWB wafers, the bonded wafers were annealed at 700ºC. To improve the bonding strength, PDA is carried out at 700ºC for 20 min in vacuum prior to bonding. Fig. 7 shows the density of micro-voids on the bonded wafers annealed at 700ºC in RTA for 1 min. As shown in Fig. 7, thinner the total thickness of Al_2O_3 is, smaller the number of micro-voids is. Finally, we have successfully reduced the micro-voids on the bonded wafer using 0.5-nm Al_2O_3/2.0-nm HfO_2 with a density of 2×10^{-3} cm^{-2}.

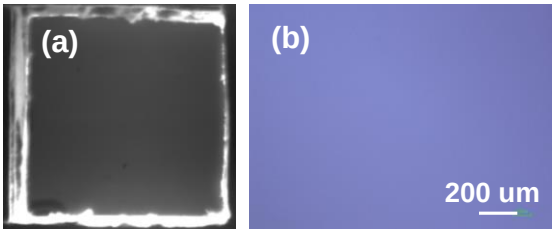

Fig. 6. IR image of the bonded wafer using (a) Al_2O_3 and (b) $Al_2O_3/HfO_2/Al_2O_3$. (c) Microscopic image of the bonded wafer using $Al_2O_3/HfO_2/Al_2O_3$ after removing top Si and SiO_2.

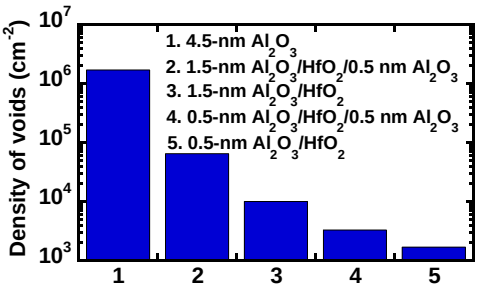

Fig. 7. Density of micro-voids on the bonded wafers annealed at 700ºC for 1 min.

3. Conclusions

To achieve a void-free direct wafer bonding, an Al_2O_3/HfO_2 bonding interface is examined. We found that the number of voids can be suppressed by introducing HfO_2 in conjunction with thinning Al_2O_3. By using a 0.5-nm Al_2O_3/2.0-nm HfO_2 interfacial layer for bonding, we successfully suppress the number of voids generated by a few orders of magnitude even when the bonded wafer is annealed at 700ºC. The presented wafer bonding is quite suitable for fabricating high-performance Si high-k MOS modulators.

Acknowledgements

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