Low Dark Current Ge Photodetector with Selectively Grown Si Capping Layer

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Abstract
Selective epitaxial growth of a Si capping layer on Ge is studied to reduce the dark current of photodetectors. Results showed that conformal 16-nm-thick Si capping layers deposited using a dichlorosilane precursor at the relatively low temperature of 670°C suppressed the dark current. Metal-semiconductor-metal photodetectors with the Si capping showed superior dark current characteristics of 1.28 nA/μm² and high quantum efficiency for irradiations of 1.31 μm and 1.55 μm.

1. Introduction
Germanium on silicon substrate is currently attracting attention for its expected application to Ge-on-Si photodetectors (PD) [1] in Si-photonics. From the viewpoint of the fabrication process in Ge-PD, Ge in itself is not a chemically stable material because its oxide GeO₂ is water soluble. This leads to an increase in surface leakage current due to the formation of localized states on the Ge surface [2]. Moreover, Ge on Si tends to be p-type polarity because any defect in Ge acts as an acceptor [3], and strong Fermi level pinning is formed at the conduction band edge of Ge due to its specific surface state [4]. Because of these two factors, the junction leakage current is considerably large. Applying the passivation/capping layer by SiGe or Si is effective to reduce the above two current components. So far, by optimizing the growth condition, a SiGe capping layer (CL) can reduce the dark current to a low level due to the formation of a Schottky barrier between SiGe and the metal electrode [5]. Although the Schottky barrier height (SBH) for the Si/Ge interface is larger than that for SiGe/Ge, it has been reported that PDs with Si-CL on Ge show a larger dark current [5]. Hence, it would be prudent to carefully investigate the Si-CL growth condition and clarify the current mechanism in PDs with Si-CL in order to further reduce the dark current in Ge PDs.

In this study, we have investigated the effect of Si-CL on selectively grown Ge on the dark current characteristics. Our findings show that the growth temperature of Si-CL remarkably affects the dark current characteristics. A flat Si-CL and a smooth interface can be obtained at relatively low growth temperature, which reduces both surface and junction leakage current.

2. Experiment
Samples were grown by reduced pressure chemical vapor deposition on a 300-mm SiO₂-patterned p-type Si (001) substrate. Germane (GeH₄) and dichlorosilane (DCS, SiH₂Cl₂) were used for the Ge and Si-CL growth, respectively, and H₂ was used for carrier gases. Before the growth, high temperature annealing was performed for native oxide removal. Then, 1-μm-thick Ge was selectively grown followed by Si-CL growth using DCS. In this experiment, we fabricated five samples under different growth conditions. First, the growth temperatures of Si-CLs were set to 670°C, 700°C, and 730°C with the thickness fixed at approximately 16 nm, and second, Si-CL thicknesses were set to approximately 10 nm and 5 nm with the growth temperature fixed at 670°C. To examine the I-V characteristics, the Ge-grown samples were covered by SiO₂ followed by TiN/Al/TiN/Ti contact formation on top of the Si-CL, as shown in Fig. 1. Optical responsivities using a metal-semiconductor-metal (MSM) PD with a ladder type electrode were measured, and transmission electron microscopy (TEM) was used to evaluate the qualities of the Si-CLs.

Fig. 1 Cross-sectional drawing of device for I-V measurement.

3. Results and discussion
We measured the I-V characteristics of the single Schottky type devices shown in Fig. 1 by biasing between the top and the backside of the Si substrate. I-V curves and dark current at 5 V are shown in Fig. 2 with changing (a) the growth temperature and (b) the thickness of the Si-CL. On the whole, up to around 3 V, the dark currents were kept at a low level, except for the 5-nm-thick Si-CL grown at 670°C. Above 3 V, differences in the dark current were observed. As the growth temperature increased and the thickness of the Si-CL decreased, the dark current increased. To clarify the components in the dark current, we measured the devices with various peripheral lengths of electrode. Figure 3 shows the dark current as a function of the peripheral length with linear fitting. From the slope and the intersection with the vertical axis, we derived the surface (d_s) and junction (d_j) components of the dark current density, as listed in Table 1. Both components increased as the growth temperature increased and the Si-CL thickness decreased.
To clarify the relationship with the band line-up, we derived the SBH between metal and Si-CL from the temperature dependence of the forward bias current [5]. The increase in both $d_s$ and $d_s$ indicates a clear relationship with the reduction of the SBH.

To clarify the behavior of the dark current characteristics, we performed TEM measurements evaluating the crystal quality. Fig. 4 shows TEM images of the Si-CL grown at different temperatures at (a) flat top regions and (b) facet regions of the Ge patterns. With regard to the interface of Si/Ge, the roughness became greater as the Si-CL growth temperature rose at both regions. The roughness became remarkably large at the facet region of the 730°C sample, probably due to the intermixing between Si and Ge during the Si-CL growth. Moreover, the Si-CL became locally thinner at the same region. The above two factors lead to the increase in $d_s$ and $d_s$ due to the formation of localized level acting as a carrier leakage pass together with the reduction of SBH.

Fig. 5 shows the optical responsivity characteristics of the MSM PD with 16-nm-thick Si-CL grown at 670°C irradiated from the top surface. Quantum efficiencies were approximately 33% and 20% for 1.31 μm and 1.55 μm, respectively, with the low dark current density of 1.28 nA/μm². These are reasonable considering the Ge thickness of 1 μm and the light shield by the top electrode.

Table 1 Surface ($d_s$) and junction ($d_s$) components of dark current densities and SBHs between metal and Si derived from temperature dependence results of I-V measurement.

<table>
<thead>
<tr>
<th>Si-cap condition</th>
<th>670°C 16 nm</th>
<th>700°C 16 nm</th>
<th>730°C 16 nm</th>
<th>670°C 10 nm</th>
<th>670°C 5 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>$d_s$(nA/μm²)</td>
<td>0.078</td>
<td>0.20</td>
<td>0.68</td>
<td>1.29</td>
<td>1.90</td>
</tr>
<tr>
<td>$d_s$(nA/μm²)</td>
<td>0.054</td>
<td>0.063</td>
<td>0.11</td>
<td>0.11</td>
<td>0.50</td>
</tr>
<tr>
<td>SBH (eV)</td>
<td>0.48</td>
<td>0.48</td>
<td>0.43</td>
<td>0.34</td>
<td>0.25</td>
</tr>
</tbody>
</table>

4. Conclusion

We investigated the effect of a Si capping layer over selective epitaxially grown Ge on the dark current characteristics of Ge-PD and found that conformal 16-nm-thick Si-CL deposited using DCS at the relatively low temperature of 670°C suppressed the dark current. Both surface and junction components of the dark current increased as the growth temperature increased and the Si-CL thickness decreased. As for the performance of MSM PDs, the low dark current of 1.28 nA/μm² and high quantum efficiency for irradiations of 1.31 μm and 1.55 μm was demonstrated.

Acknowledgements

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References