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The influence of III-V on insulator structure on quantum well intermixing

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Abstract **We have investigated the impact of a III-V on insulator structure on quantum well intermixing for active/passsive integration on the III-V CMOS photonics platform. It was found that the speed of the intermixing in the III-V on insulator structure was much slower than that in bulk III-V wafers. By applying the intermixing at the appropriate condition, we achieved approximately 100nm wavelength shift in photoluminescence peak by qunatum well intermixing on the III-V-OI wafer.**

1. Introduction

Electronic-photonic integrated circuits (EPICs) have recently attracted much attention for off-chip and on-chip optical interconnects. We have proposed the III-V CMOS photonics [1] using III-V on insulator (III-V-OI) wafer as a platform for EPIC which enables drastic side reduction of conventional InP-based photonics owing to the strong optical confinement. In addition to the benefit for photonics, III-V semiconductors such as InGaAs are expected as alternative channel materials to Si for metal-oxide-semiconductor (MOS) transistor application because of their high electron mobility. We have demonstrated InP-based photonic-wire waveguide components including micro-bends, arrayed waveguide gratings [2], grating couplers [3], optical switches [4], and InGaAs PDs [5] on the III-V CMOS photonics. High-performance InGaAs MOSFETs on the III-V-OI wafer have also been demonstrated [6, 7]. To integrate those devices monolithically on the same III-V-OI wafer, as shown in Fig.1, we have demonstrated multi-bandgap III-V-OI by applying quantum well intermixing (QWI) [8] to a III-V bulk wafer before the direct wafer bonding (DWB) process. However, the QWI after bonding is preferable in terms of process flexibility.

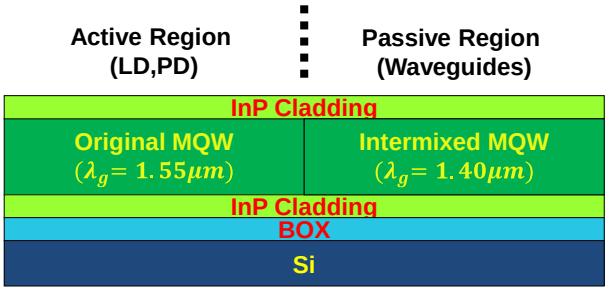

Fig.1 Schematic of active/passive integration on multi-bandgap III-V-OI wafer fabricated by QWI.

In this study, we have investigated a fabrication procedure of a multi-bandgap III-V-OI wafer by applying the QWI process to III-V-OI wafers after the DWB process. By exploring the impact of the III-V-OI structure on the QWI, we have achieved the photoluminescence (PL) peak shift of approximately 100 nm on the III-V-OI wafer.

2. Experiments

We prepared III-V wafers by the epitaxial growth on an InP substrate. The active region consists of InGaAsP-based multi quantum well (MQW) layers with total thickness of 90 nm sandwiched by 80-nm-thick InP cladding layers. A layer of InGaAs was also grown as an etching stop layer.

The upper part of Fig. 2 shows the process flow of the III-V-OI wafers by DWB. After pre-cleaning the III-V wafer and a SiO_2/Si wafer, 2.7-nm-thick Al_2O_3 is deposited on these wafers by atomic layer deposition (ALD). Then, these wafers were manually bonded and annealed in 350°C for 1 h under 1000N pressure. Finally the InP substrate and etch stop layers were removed by selective wet etching.

The lower part of Fig. 2 shows the schematic process flow of ion-implantation-induced QWI [9]. The III-V-OI wafer was pre-cleaned and masked with 0 to 5-nm-thick Al_2O_3 by ALD. Then, P ions were implanted with 3 keV into the top InP layer to generate point defects, and finally the MQW was intermixed through the following rapid thermal annealing (RTA) in 650 °C. The intermixing was also carried out for the MQW on InP wafer with the same condition. The bandgap shift in the MQW layer was evaluated by PL measurement at room temperature.

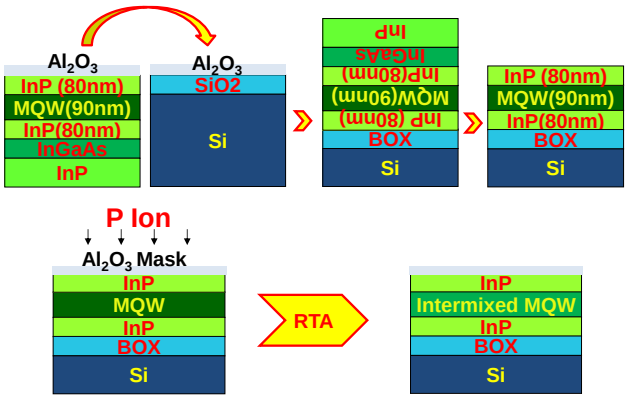

Fig.2 Fabrication process of multi-bandgap III-V-OI wafer by DWB and QWI.

3. Results

Fig. 3 shows the normalized PL spectra of the III-V-OI samples with 1-nm-thick Al_2O_3 mask before and after QWI by annealing at 650 °C for 32 min. It is shown that the PL peak is shifted by approximately 100 nm by QWI for the bonded III-V-OI wafer. It is worth noting that the full width half maximum (FWHM) is not changed through QWI. Fig. 4 shows the ratio of PL peak intensity of the intermixed MQWs on the III-V-OI wafer and bulk InP wafer. We observed no significant degradation in the PL intensity of the III-V-OI wafer as compared with the InP wafer.

Fig. 5 shows the PL peak shifts of the III-V-OI and bulk wafers as a function of the annealing time. The thickness of

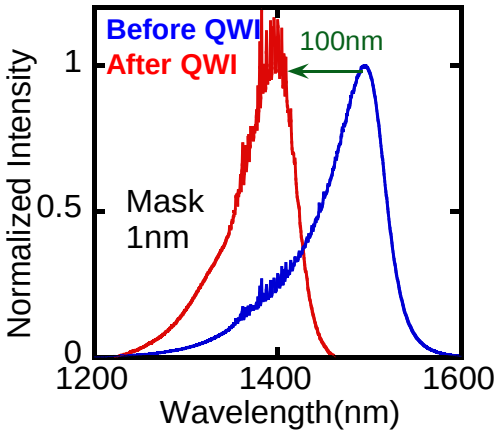

Fig. 3 PL spectra of III-V-OI before and after QWI by annealing at 650 °C for 32min.

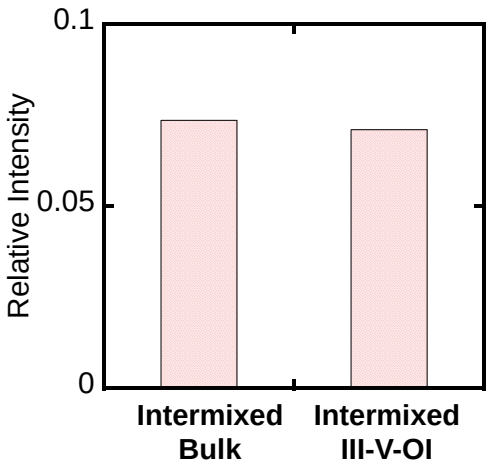

Fig. 4 Relative intensity of the PL peak of intermixed bulk and III-V-OI samples, compared with unintermixed samples of each conditions

the Al_2O_3 mask in the QWI process was 2 nm at this time. It was found that the intermixing evolved more slowly on the III-V-OI wafer than on the InP bulk wafer.

4. Discussions

As shown in Fig. 5, the speed of intermixing on the III-V-OI wafer was lower than that on the InP bulk wafer. We consider this difference can be attributed to three factors peculiar to the III-V-OI wafers: the temperature variation, the thermal stress, and the buried oxide (BOX).

In this study we investigate the impact of the temperature variation due to the presence of the BOX layer. If the slow intermixing speed is fully attributed to the temperature difference, the identical PL shift can be obtained even on the III-V-OI wafer when the annealing temperature is increased to compensate the temperature difference during RTA. Thus, we examined the PL shift of the III-V-OI wafer by annealing at higher temperatures as show in Fig. 5. When the QWI was performed at 700 °C, the III-V-OI sample exhibited the same PL shift as the bulk sample at 4 min annealing. However, the evolution of the PL shift on the III-V-OI wafer dissociated from that on the bulk wafer after 4 min annealing. Therefore we conclude the lower

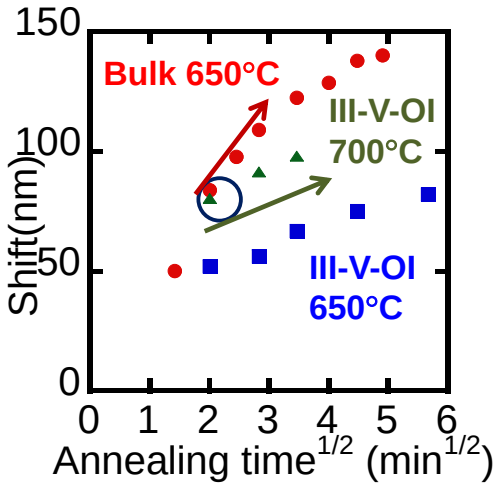

Fig. 5 The PL peak shift as a function of the annealing time at annealing for the different substrates and QWI temperature

intermixing speed on the III-V-OI wafer should be attributed to the other factors; the thermal stress and the buried oxide. There are some reports that on SOI, the diffusion of dopants is affected by stress and buried oxides [10,11]. Although we can expect the similar effect in the III-V-OI wafer, we still need further investigations to clarify the impact of these two factors on QWI.

5. Conclusions

We have investigated the QWI process on III-V-OI wafers. We have found that the evolution of QWI on the III-V-OI was slower than on the InP bulk wafer. By applying the longer annealing time for QWI, we achieved the PL peak shift of approximately 100 nm even on the III-V-OI wafer. Thus, we successfully demonstrated the feasibility of the active/passive integration on the III-V-OI wafer through QWI, which is an attractive process for large-scale photonic integration on the III-V CMOS photonics.

Acknowledgements

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