Temperature-Dependent Minority Carrier Lifetime of Crystalline Silicon Wafers Passivated by High Quality Amorphous Silicon Oxide

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Abstract

We measured the temperature dependence of the minority carrier effective lifetime of passivated crystalline silicon. Analysis of the sample with a best passivation layer revealed the very small surface recombination velocity of 0.35 cm/s. The temperature dependence for this well-passivated sample is substantially determined by the bulk recombination in c-Si. On the other hand, the samples in which interface defect density was increased by a high temperature annealing exhibited a different temperature dependence. Our device simulations suggest that interface defect distribution and valence band offset significantly affect the temperature dependence.

1. Introduction

The surface passivation of crystalline silicon (c-Si) is a crucial issue for high-efficiency c-Si solar cells. Amorphous silicon related materials, such as hydrogenated amorphous silicon (a-Si:H) and hydrogenated amorphous silicon oxide (a-Si_{1-x}O_x:H) are very good passivation materials, and they are commonly used for passivation layer of heterojunction crystalline silicon solar cells [1-3]. The state-of-the-art amorphous silicon related passivation layer has been intensively investigated by several research groups [4-6] and modeling of the recombination at the a-Si:H/c-Si interface was also reported [7]. Device simulations of heterojunction crystalline silicon solar cells were also investigated [8, 9], however, the information of the passivation layer/c-Si interface is still limited. Therefore, further investigation of the recombination mechanism at the interface is required.

To evaluate the surface passivation quality, the surface recombination velocity, which is calculated by minority carrier effective lifetime, is investigated [10]. Injection-dependent lifetime measurements [11] are generally performed at room temperature. For the investigation of the c-Si bulk properties, the temperature-dependent lifetime measurement was employed [12]. This method enables to determine the defect levels. In case of high quality c-Si wafers, we can assume one discrete defect level in the bulk c-Si. On the other hand, the defect levels at the passivation layer/c-Si interface are distributed continuously. Therefore, the temperature dependence of surface recombination of the crystalline silicon should be different from that of the bulk c-Si, suggesting that temperature dependence of effective lifetime provides the information of the interface.

In this study, we investigated the temperature dependence of the effective lifetime of the c-Si wafer with high-quality a-Si_{1-x}O_x:H passivation layer on the both sides.

2. Experiment

The c-Si wafer used in this work was float-zone double-side-polished n-type (phosphorus-doped) c-Si wafer. The thickness and resistivity of the c-Si wafer were 280 µm and 3.0 Ω cm, respectively. They were dipped in hydrofluoric acid (HF) solution (5%) to remove the native oxide before deposition of the passivation layers. We used intrinsic (i-type) a-Si_{1-x}O_x:H with an oxygen content of about 5 -10% as a passivation layer. The thickness of the passivation layer is about 20 nm. The passivation layer was deposited by very high-frequency plasma-enhanced chemical vapor deposition (VHF-PECVD) with a frequency of 60 MHz. The substrate surface temperature was 210 °C. Mixtures of silane (SiH₄), hydrogen (H₂) and carbon dioxide (CO_2) were used as source gases. The sample structure is shown in Fig. 1. The sample was annealed after the film deposition to improve the passivation quality. Annealing was carried out in the forming gas ambient at 200 °C for 30 min.

Temperature dependence of the minority carrier effective lifetime was measured by quasi steady-state photosystem conductance (QSSPC) (Sinton Consulting WCT-120) equipped with a substrate heater. The temperature range was from 60 °C to 180 °C. The measured effective lifetime was analyzed by SRH recombination model and one dimensional device simulator. After the measurement, we performed high temperature annealing of the sample to increase the interface defect density. It is possible to increase the interfacial defects by annealing at the temperature above the film deposition temperature, because of desorption of hydrogen from the passivation layers. The annealing was carried out in the forming gas ambient at 300 °C to 500 °C for 5 min. We measured the effective lifetime after each annealing.



Fig. 1 Structure of the sample used in this work

3. Results and discussions

Fig. 2 shows the temperature dependence of the effective lifetime of the sample annealed at various temperatures. The defect energy level in the c-Si and the bulk lifetime were estimated from the measurement result of the sample annealed at 200 °C. For this annealing condition, the effective lifetime is significantly high. Therefore, the influence of the surface recombination is extremely small and we can neglect its temperature dependence. We obtained very good fitting by using SRH model assuming a single defect level as shown in the Fig. 2. The estimated parameters were the bulk lifetime (τ_b) of 18 ms, the defect energy level (E_t) of 0.33 eV, and the surface recombination velocity (S) of 0.35 cm/s.

Increasing the surface defects by high temperature annealing leads to the decrease of the minority carrier effective lifetime. As well as the reduction of the effective lifetime, tendency of the temperature dependence was greatly changed. It suggests that the temperature dependence of surface recombination is very different from the temperature dependence of the bulk recombination. Thus, SRH model assuming a single defect level cannot provide good fitting for the sample annealed at above 300 °C.

There are two reasons of the significant change in the temperature dependence. One reason is the continuous distribution of the defect level. After annealing at above 300 °C, defect density at the interface increased, resulting in the increase of the proportion of surface recombination to total recombination. When the surface recombination is dominant, temperature dependence reflects temperature dependence of the surface recombination. The other reason is the bandgap reduction. The higher temperature annealing decrease the bandgap of $a-Si_{1-x}O_x$:H. The reduction of the bandgap leads to the change of valence band and conduction band offset. Our device simulation revealed that valence band offset significantly affects the temperature dependence of the minority carrier lifetime.



Fig. 2 Temperature dependence of minority carrier effective lifetime for each annealing temperature. The solid lines in this figure are the calculated effective lifetime considering only the temperature dependence of the bulk c-Si.

4. Conclusions

We measured minority carrier effective lifetime of c-Si wafer passivated by high-quality i-a-Si_{1-x}O_x:H. After 200 °C annealing, the sample showed very small surface recombination velocity of 0.35 cm/s. The bulk lifetime and defect level were also found to be 18 ms and 0.33 eV, respectively. In addition, we also found that the surface recombination caused by the defect at the passivation layer/c-Si interface shows different temperature dependence from c-Si bulk recombination. Our analysis and device simulation suggest that the temperature dependence of the effective lifetime is strongly influenced by defect distribution at the interface and valence band offset.

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