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Atomically-thin semiconductors

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Abstract

A atomically thin two-dimensional chalcogenides are ideal channel materials for the ultimate atomic electronics. Using atomic-scale thin film of transition metal dichalcogenides (TMDs), we have developed semiconducting channel for future electronics. We investigated transport properties, particularly scattering property in field effect transistors (FETs). In this transport experiment, it is found that the carrier scattering from interfacial Coulomb impurities is greatly intensified in extremely thinned channels, resulting from shortened interaction distance between impurities and carriers.

1. Introduction

Transition metal dichalcogenides (TMDs) with the common formula MX_2, where M stands for a transition metal from group IV-VII (M = Mo, W, Nb, Re, and so on) and X is a chalcogen element (S, Se, Te), is a well-known class of layered composite materials. In these layered materials, a hexagonally packed layer of M atoms is sandwiched between two layers of X atoms, and the triple layers stack together via weak van der Waals forces, which facilitate cleavage of the bulk crystals to form individual 2D flakes along each triplet of layered structures.

Using atomic-scale thin film of metal dichalcogenides layered material, we have developed semiconducting channel for future electronics. We investigated optical properties and transport properties, particularly scattering property of carrier transport in field effect transistors (FETs). In this transport experiment, we characterized one of the important properties of the TMDs for electronics.

2. General Instructions

A long-standing puzzle is the low carrier mobility (μ) in them as compared with corresponding bulk structures, which constitutes the main hurdle for realizing high-performance FETs. To address this issue, we perform a combined experimental and theoretical study on atomically thin MoS_2 FETs with varying the number of MoS_2 layers (NLs).

The experimental setup is as follows. The MoS_2 flakes, from 1 to 24 layers, were prepared by micromechanical cleavage from natural MoS_2 crystals and were transferred to oxygen plasma cleaned SiO_2/Si wafers (p-type, ρ < 8 μ□ cm). Figure 1 shows optical images of fabricated FETs with multiple electrodes based on MoS_2 flakes with consecutive NLs from 2 to 6. The thickness information is double checked by optical contrast and interference Raman spectroscopy. The large sample dimensions enable us to fabricate multiple electrodes on devices to exclude contact resistance (Rc). Also, the consecutive NLs on the same substrate allow for a fair comparison of device performance because of nearly identical external conditions. The close locations among flakes make it possible to identify NL quickly from optical contrast. For electrical measurement, all flakes are etched into rectangular bars with typical channel width (W) and length (L) 1–3 and 5–20 μm, respectively.

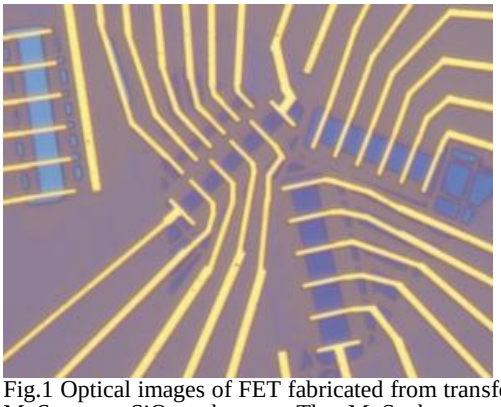

Fig.1 Optical images of FET fabricated from transferred MoS_2 onto SiO_2 substrate. The MoS_2 have various numbers of layers from 2 to 6.

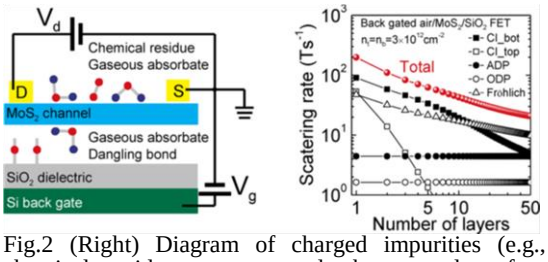

Fig.2 (Right) Diagram of charged impurities (e.g., chemical residues, gaseous adsorbates, and surface dangling bonds) located on the top and bottom channel surfaces, which are the leading scatterers in ultrathin channels. (Left) Calculated scattering rates for a back-gated air/MoS2/SiO_2 structure assuming nt = nb = 3×10^{12} /cm^2.

Experimentally, an intimate μ−NL relation is observed with a 10-fold degradation in μ for extremely thinned monolayer channels. To accurately describe the carrier scattering process and shed light on the origin of the thinning-induced mobility degradation, a generalized Coulomb scattering model is developed with strictly considering FET configurative conditions, that is, asymmetric dielectric environments and lopsided carrier distribution. We reveal that the carrier scattering from interfacial Coulomb impurities (e.g., chemical residues, gaseous adsorbates, and surface dangling bonds) is greatly intensified in extremely thinned channels, resulting from shortened interaction distance between impurities and carriers. Such a

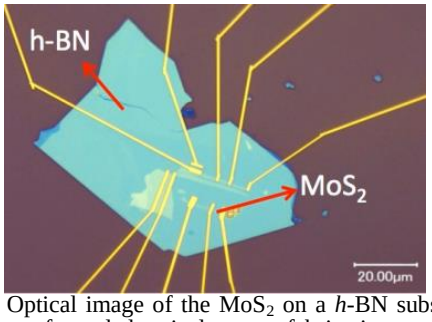

Fig.3 Optical image of the MoS_2 on a *h*-BN substrate after transfer and electrical contact fabrication.

pronounced factor may surpass lattice phonons and serve as dominant scatterers. This understanding offers new insight into the thickness induced scattering intensity, highlights the critical role of surface quality in electrical transport, and would lead to rational performance improvement strategies for future atomic electronics.

As a result of the above experimental and theoretical characterization, it is found that the atomically thin film needs to be combined with atomically flat substrate with the non-polar surface to get the intrinsic transport. Thus, we fabricated MoS_2 field-effect transistors on crystalline hexagonal boron nitride (*h*-BN) and SiO_2 substrates. Temperature dependence of these transistors shows distinct weak temperature dependence of the MoS_2 devices on *h*-BN substrate. At the room temperature, mobility enhancement and reduced interface trap density of the single and bilayer MoS_2 devices on *h*-BN substrate further indicate that reducing substrate traps is crucial for enhancing the mobility in atomically thin MoS_2 transistors. Furthermore, we fabricated a field effect transistor with a novel combination of graphene and nano-sheet to realize atomically thin film hetero-structure. A high-quality $HCa_2Nb_3O_{10}$ (HCNO) nanoflake (dielectric constant ~9.1) consisting of high-k perovskite nanosheets is adopted as a gate dielectric for graphene-based electronics. A dual-gated device was physically constructed by directly dry-transferring a 22-nm-thick HCNO nanoflake as a top gate dielectric onto graphene. The fabricated graphene field-effect transistor could be operated at biases <1.5V with a gate leakage below 1 pA. The top-gate capacitance and mobility of the dual-gated graphene device at room temperature were estimated to be 367 nF/cm^2 and 2500 cm^2/Vs, respectively. These results show that HCNO can be employed as an alternative dielectric for graphene-based electronics.

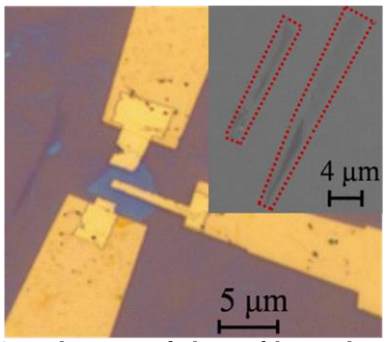

Fig.4 Optical image of the as-fabricated graphene FET with HCNO gate-insulator. Inset shows an optical image of the monolayer graphene used to fabricate the FET. The stacked structure was fabricated by dry-transfer processes to obtain HCNO-on-graphene FETs, where the HCNO nanoflake was treated as the top-gate dielectric.

3. Conclusions

We provide an in-depth understanding on the carrier transport behavior for common trilayer structured FETs, especially on the dominant scattering mechanisms at atomic scale. As technological guidance, slightly thick channels, rather than monolayers, are more robust to extrinsic scattering and thus hold more favorable application promises. In addition, a clean interface is the most crucial in realizing high-performance ultrathin-body FETs in atomic electronics.

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