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Template-Assisted Selective Epitaxy (TASE) of III-V Nanoscale Devices for Heterogeneous Integration with Si

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Abstract

III-V nanoscale devices were monolithically integrated on silicon-on-insulator substrates by template-assisted selective epitaxy (TASE) using metal organic chemical vapor deposition. The benefit of TASE is demonstrated by the fabrication of lateral InAs multiple gate field effect transistors (FETs) as well as by vertical InAs-Si gate-all-around p-type Tunnel FETs.

1. Introduction

III-V compound semiconductors are considered to extend the logic device roadmap as conventional silicon (Si) field-effect transistor (FET) scaling is fast approaching its limits. As alternative channel material, they are well positioned to deliver performance increase for logic switching devices due to their higher electron mobility and saturation velocities compared to Si [1]. Furthermore, the constraints of device scaling demand transistor channels with a three-dimensional structure, such as FinFETs or nanowire (NW) FETs, to achieve future performance needs. Another key challenge of scaling is to further reduce the supply voltage to decrease the power consumption. This could be addressed by Tunnel FETs (TFETs) which make use of band-to-band tunneling to inject charge carriers into the channel and thus enable sub-k_BT/q switching and low-voltage operation [2]. Recent TFET results indicate that III-V compound semiconductors and their heterostructures are crucial materials for achieving the required device performance. In particular, III-V heterostructures allow engineering of the effective tunnel barrier and enable higher on-currents compared to TFETs based on Si. Although there has been significant scientific and technical progress achieved in III-V MOSFETs and TFETs, the monolithic integration of III-V materials on Si is key for their future success. It is therefore crucial to find methods to integrate high-quality III-V materials with established Si technology in an economically viable way, compatible with standard CMOS processes.

2. Integration of III-V Semiconductors on Silicon

The monolithic integration of III-V's on Si is a major challenge because of the large mismatch in lattice distance and thermal expansion coefficient as well as the anti-phase boundaries resulting from the semi-ionic nature of the III-V crystal structure. To date the most successful integration schemes are based on direct wafer bonding [3] and selective growth approaches using dielectric masks [4-6] such as, e.g., aspect ratio trapping (ART). ART makes use of selective growth in trenches where threading dislocations are diverted to the sidewalls perpendicular to the trench but not necessarily along the trench [4]. Reducing the mask opening to below 100 nm, threading dislocations and anti-phase boundaries can be avoided as shown by defect-free hetero-interfaces for NWs on Si [5,6]. However, while attractive for their ease of fabrication catalyst-free grown NWs have certain limitations: the growth parameter window is rather tight, growth has been shown only in (111) direction and growth regularly results in non-intentional core–shell structures when attempting axially modulated NWs. We have developed a new process for monolithic integration of III–V NWs on silicon called template-assisted elective epitaxy (TASE) that avoids these shortcomings [7-9]. In TASE the nanostructure is seeded on a Si area of below 100 nm and the growth is guided within SiO_2 nanotube templates, which determine the shape and direction of the nanostructure crystal as shown in Fig. 1. This method allows the epitaxial growth of vertical NWs [7,8] as well as lateral complex nanostructures like constrictions along a nanostructure and NW cross junctions [9] monolithically integrated on Si. We have also shown that with TASE nanostructures on Si substrates of varying crystallographic orientations (e.g. (111), (110), and (100)), including nanocrystalline Si can be grown. The resulting nanostructures are single-crystalline, free from threading dislocations, and with an orientation and dimension directly given by the shape of the template.

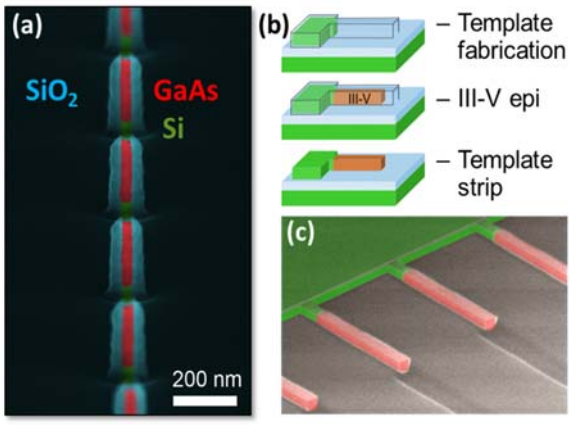

Fig. 1 (a) SEM of vertical GaAs NWs epitaxially grown on Si within SiO_2 nanotube templates. (b) Schematic illustration of lateral TASE process. (c) SEM of lateral InAs NWs epitaxially grown on Si as shown in (b) after removal of template.

3. Lateral InAs Multiple-Gate MOSFETs

Based on InAs NWs grown by lateral TASE multiple-gate (MuG)-FETs were fabricated as shown in Fig. 2. They comprise up to 10 parallel InAs nanowire channels of 23 nm thickness and various width between 25 and 55 nm. The SiO_2 template was removed in diluted HF and an $Al_2O_3/HfO_2/TiN$ gate stack was deposited by atomic layer deposition (ALD) with an equivalent effective oxide thickness (EOT) of 1.2 nm. The 20-nm-thick gate metal was patterned by wet etching and the source drain contacts were formed by Ni/Au metallization. The on-current, I_{on} at V_{DS}=0.5 V is 500 µA/µm using the device width for normalization. A maximum transconductance of 0.82 mS/µm at 0.5 V is achieved, which is comparably high considering the large contact and access resistances observed (resistivity: ~ 2.90 mΩ-cm, contact resistance: 500 Ω, and specific contact resistivity: ~ $9.5x10^{-8}$ Ω-cm^2).

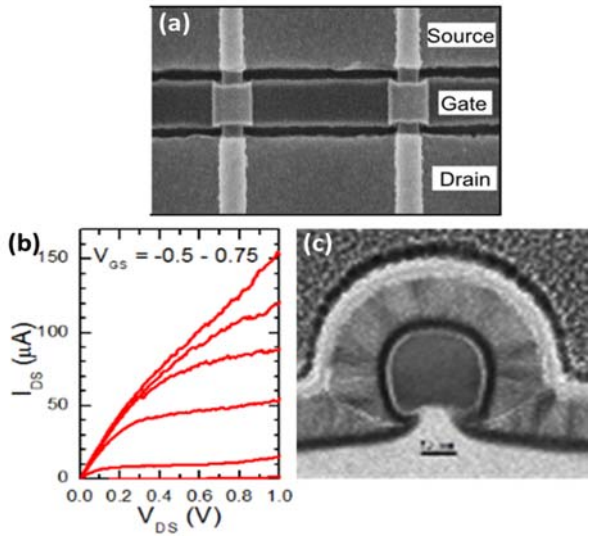

Fig. 2 (a) Top-view SEM of an InAs NW MuG-FET. (b) Output characteristics of a 25 nm wide, 23 nm high InAs NW MuG-FET. (c) TEM cross-section image of 25 nm wide, 23 nm high InAs NW.

4. Vertical InAs-Si Nanowire Tunnel FETs

The TASE approach has been also applied to fabricate vertical InAs-Si p-type NW TFETs on Si as shown in Fig. 3(a) [10]. A process flow to fabricate vertical TFETs was developed and significantly improved by (1) optimizing the InAs NW growth process (growth temperature, V/III ratio and precursor flow) for high yield and material quality, (2) using inorganic TEOS spacer layers, (3) using ALD for depositing the metal gate, and (4) scaling the EOT from 2.7 to 1.5 nm. A gate-all-around ALD gate stack of Al_2O_3/HfO_2 (2.2 nm/2.4 nm) and 20 nm TiN is deposited at 250ºC and 300ºC, respectively. The gate is patterned and isolated from the source using TEOS and lift-off is used to fabricate Ni/Au top contacts. The output and transfer characteristics are shown in Fig. 3(b) and (c). The TFETs exhibit a good device performance with on-currents, I_{on} of 6 µA/µm at $|V_{GS}| = |V_{DS}| =$ 1 V and a room temperature subthreshold swing (SS) of ~160 mV/dec over at least three orders of magnitude of current. Furthermore, an I_{on}/I_{off} ratio of ~10^6 was achieved. Temperature dependent measurements indicate that SS is limited by traps.

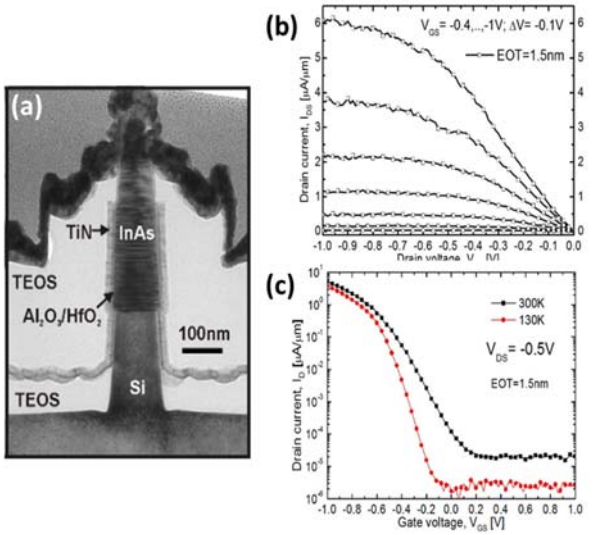

Fig. 3 (a) TEM cross-section of a vertical InAs-Si NW TFET. (b) Output characteristics and (c) I_{DS} vs. V_{GS} at V_{DS} = -0.5 V measured at 300 and 130 K of an InAs-Si NW TFET with a NW diameter of 100 nm and with EOT = 1.5 nm.

3. Conclusions

We have demonstrated a CMOS compatible heterogeneous approach to integrate lattice mismatched materials on Si and SOI substrates. TASE allows the monolithic integration of lateral as well as vertical III-V nanostructures with complex shape by epitaxial growth on Si. Well performing multiple-gate lateral InAs NW FETs as well as vertical InAs-Si heterostructure NW TFETs have been demonstrated. The results indicate the high potential of TASE for III-V on Si co-integration for electronic as well as opto-electronic devices.

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